


Quanta Project Name: GM7B

Dell Project Name: Shatner

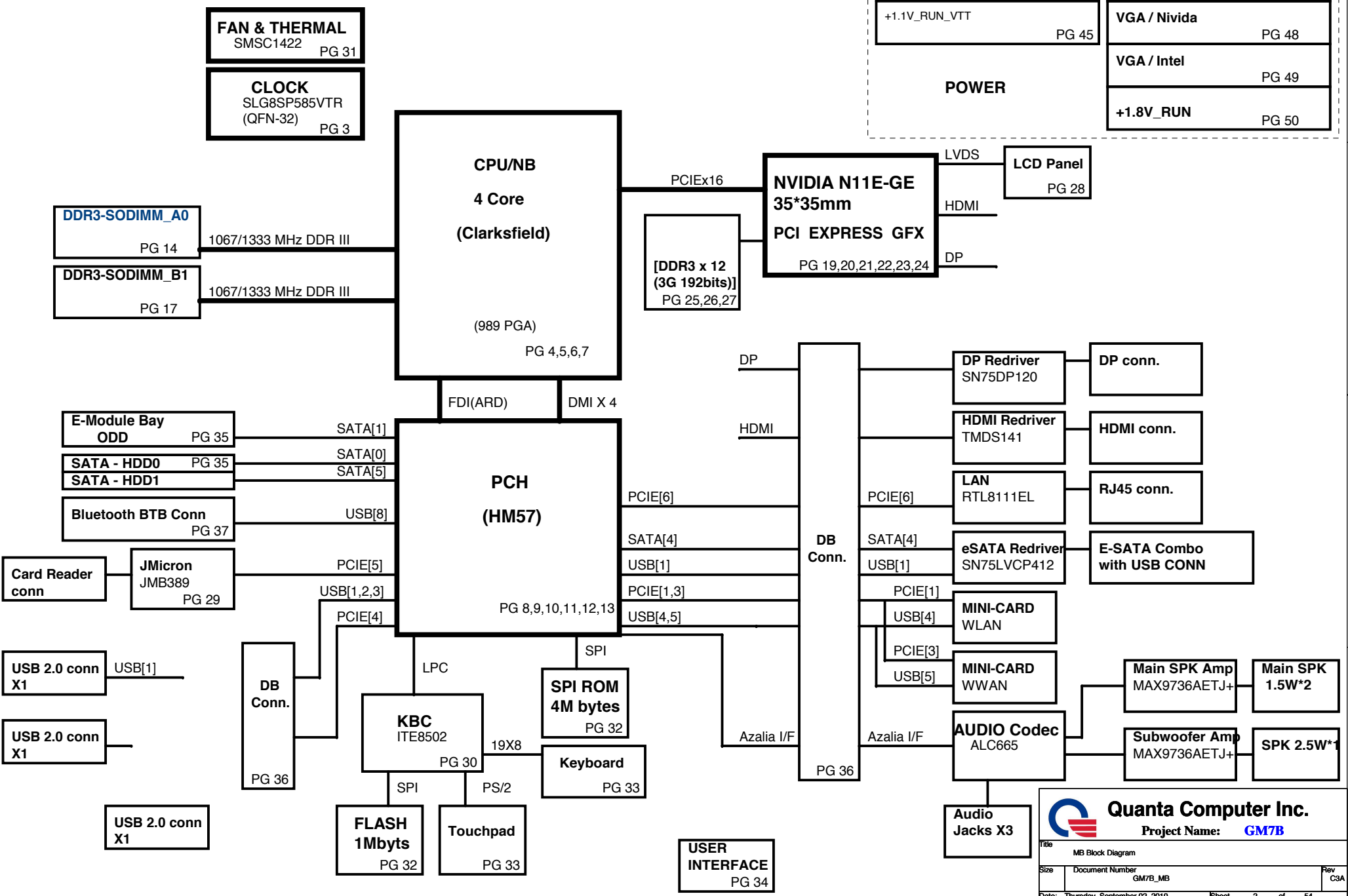
A00(QT) Stage

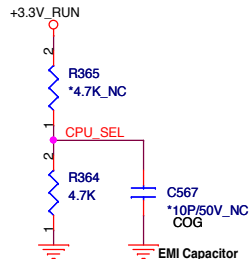
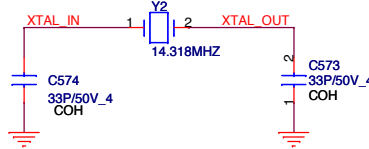
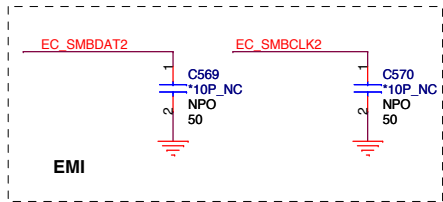
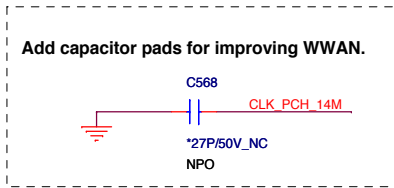
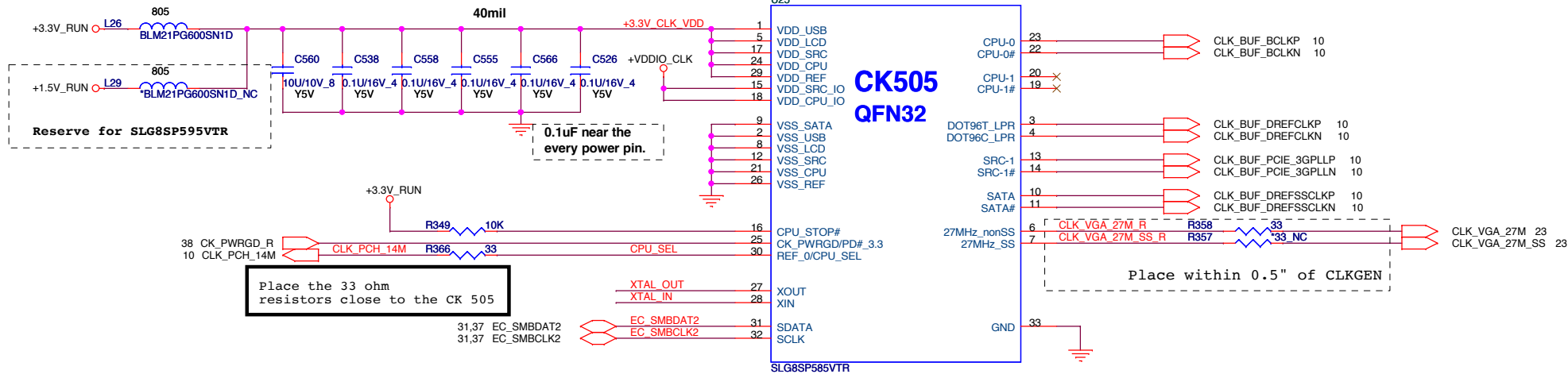
BOARD REV : C

2010-08

		Quanta Computer Inc.	
		Project Name: GM7B	
Title CoverPage			
Size	Document Number GM7B_MB		Rev C3A
Date: Thursday, September 02, 2010 Sheet 1 of 54			

System Block Diagram of GM7B

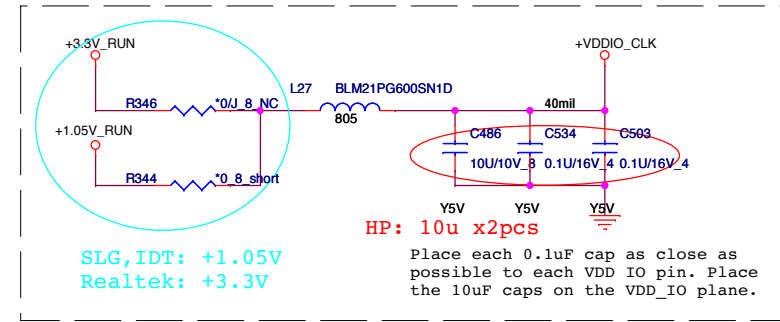




PIN 30	CPU_0	CPU_1
0 (default)	133MHz	133MHz
1 (0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet(V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet(V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

**Realtek: 0.1uFx3pcs, 22uFx1pcs
IDT: 0.1uFx2pcs, 10uFx1pcs**



+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V, Max 3.465V.
Realtek date sheet(V1.2) P11: Min 1.05V, Max 3.3V.
IDT date sheet(V0.7) P10: Min 0.9975V, Max 3.465V.

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

U39C

14 M_A_DQ[8:0] M_A_DQ0 A10 SA_DQ[0] M_A_DQ1 C10 SA_DQ[1] M_A_DQ2 C7 SA_DQ[2] M_A_DQ3 A7 SA_DQ[3] M_A_DQ4 B10 SA_DQ[4] M_A_DQ5 D10 SA_DQ[5] M_A_DQ6 E10 SA_DQ[6] M_A_DQ7 A8 SA_DQ[7] M_A_DQ8 D8 SA_DQ[8] M_A_DQ9 E10 SA_DQ[9] M_A_DQ10 E8 SA_DQ[10] M_A_DQ11 E7 SA_DQ[11] M_A_DQ12 E9 SA_DQ[12] M_A_DQ13 B7 SA_DQ[13] M_A_DQ14 E7 SA_DQ[14] M_A_DQ15 C6 SA_DQ[15] M_A_DQ16 H10 SA_DQ[16] M_A_DQ17 S8 SA_DQ[17] M_A_DQ18 K7 SA_DQ[18] M_A_DQ19 J8 SA_DQ[19] M_A_DQ20 G7 SA_DQ[20] M_A_DQ21 G10 SA_DQ[21] M_A_DQ22 J7 SA_DQ[22] M_A_DQ23 I7 SA_DQ[23] M_A_DQ24 L7 SA_DQ[24] M_A_DQ25 M6 SA_DQ[25] M_A_DQ26 L8 SA_DQ[26] M_A_DQ27 L9 SA_DQ[27] M_A_DQ28 L6 SA_DQ[28] M_A_DQ29 K6 SA_DQ[29] M_A_DQ30 N8 SA_DQ[30] M_A_DQ31 P9 SA_DQ[31] M_A_DQ32 A9 SA_DQ[32] M_A_DQ33 A5 SA_DQ[33] M_A_DQ34 A6 SA_DQ[34] M_A_DQ35 A7 SA_DQ[35] M_A_DQ36 A8 SA_DQ[36] M_A_DQ37 A9 SA_DQ[37] M_A_DQ38 A10 SA_DQ[38] M_A_DQ39 A11 SA_DQ[39] M_A_DQ40 A12 SA_DQ[40] M_A_DQ41 A13 SA_DQ[41] M_A_DQ42 A14 SA_DQ[42] M_A_DQ43 A15 SA_DQ[43] M_A_DQ44 A16 SA_DQ[44] M_A_DQ45 A17 SA_DQ[45] M_A_DQ46 A18 SA_DQ[46] M_A_DQ47 A19 SA_DQ[47] M_A_DQ48 A20 SA_DQ[48] M_A_DQ49 A21 SA_DQ[49] M_A_DQ50 A22 SA_DQ[50] M_A_DQ51 A23 SA_DQ[51] M_A_DQ52 A24 SA_DQ[52] M_A_DQ53 A25 SA_DQ[53] M_A_DQ54 A26 SA_DQ[54] M_A_DQ55 A27 SA_DQ[55] M_A_DQ56 A28 SA_DQ[56] M_A_DQ57 A29 SA_DQ[57] M_A_DQ58 A30 SA_DQ[58] M_A_DQ59 A31 SA_DQ[59] M_A_DQ60 A32 SA_DQ[60] M_A_DQ61 A33 SA_DQ[61] M_A_DQ62 A34 SA_DQ[62] M_A_DQ63 A35 SA_DQ[63]

DDR SYSTEM MEMORY - A

P298927-3641-01F

14 M_A_BS#0 AC3 SA_BS[0] 14 M_A_BS#1 A82 SA_BS[1] 14 M_A_BS#2 U7 SA_BS[2] 14 M_A_CAS# AE1C SA_CAS# 14 M_A_RAS# AB3C SA_RAS# 14 M_A_WE# AE9C SA_WE#

SA_CK[0] AA6 M_A_CLK0 14 SA_CK[0] AA7 M_A_CLK0# 14 SA_CK[0] A7 M_A_CKE0 14 SA_CK[1] Y6 M_A_CLK1 14 SA_CK[1] Y5 M_A_CLK1# 14 SA_CK[1] P6 M_A_CKE1 14 SA_CS#0 AE2 M_A_CS#0 14 SA_CS#1 AE8 M_A_CS#1 14 SA_ODT[0] AD8 M_A_ODT0 14 SA_ODT[1] AE9 M_A_ODT1 14 SA_DM[0] B9 M_A_DM0 M_A_DM[7:0] 14 SA_DM[1] D7 M_A_DM1 SA_DM[2] H7 M_A_DM2 SA_DM[3] M7 M_A_DM3 SA_DM[4] AS6 M_A_DM4 SA_DM[5] AM7 M_A_DM5 SA_DM[6] AN10 M_A_DM6 SA_DM[7] AN13 M_A_DM7 M_A_DQS#0 C9 M_A_DQS#0 M_A_DQS#7:0] 14 M_A_DQS#1 F9 M_A_DQS#1 M_A_DQS#2 J9 M_A_DQS#2 M_A_DQS#3 N9 M_A_DQS#3 M_A_DQS#4 AH7 M_A_DQS#4 M_A_DQS#5 AP11 M_A_DQS#5 M_A_DQS#6 AP11 M_A_DQS#6 M_A_DQS#7 AL13 M_A_DQS#7 M_A_DQS#0 C8 M_A_DQS#0 M_A_DQS#7:0] 14 M_A_DQS#1 F9 M_A_DQS#1 M_A_DQS#2 J9 M_A_DQS#2 M_A_DQS#3 N9 M_A_DQS#3 M_A_DQS#4 AH8 M_A_DQS#4 M_A_DQS#5 AN11 M_A_DQS#5 M_A_DQS#6 AN13 M_A_DQS#6 M_A_A[0] Y3 M_A_A0 M_A_A[1] W1 M_A_A1 M_A_A[2] AA6 M_A_A2 M_A_A[3] AA3 M_A_A3 M_A_A[4] V1 M_A_A4 M_A_A[5] V8 M_A_A5 M_A_A[6] T1 M_A_A6 M_A_A[7] Y9 M_A_A7 M_A_A[8] U6 M_A_A8 M_A_A[9] AD4 M_A_A9 M_A_A[10] U3 M_A_A10 M_A_A[11] T3 M_A_A11 M_A_A[12] T3 M_A_A12 M_A_A[13] T3 M_A_A13 M_A_A[14] T3 M_A_A14 M_A_A[15] V9 M_A_A15

17 M_B_BS#0 AB1 SB_BS[0] 17 M_B_BS#1 W5 SB_BS[1] 17 M_B_BS#2 D7 SB_BS[2] 17 M_B_CAS# AC5C SB_CAS# 17 M_B_RAS# Y7C SB_RAS# 17 M_B_WE# AC6C SB_WE#

U39D

M_B_DQ0 B5 SB_DQ[0] M_B_DQ1 A5 SB_DQ[1] M_B_DQ2 C3 SB_DQ[2] M_B_DQ3 B3 SB_DQ[3] M_B_DQ4 E4 SB_DQ[4] M_B_DQ5 A6 SB_DQ[5] M_B_DQ6 A4 SB_DQ[6] M_B_DQ7 C4 SB_DQ[7] M_B_DQ8 D1 SB_DQ[8] M_B_DQ9 D2 SB_DQ[9] M_B_DQ10 E1 SB_DQ[10] M_B_DQ11 E1 SB_DQ[11] M_B_DQ12 C2 SB_DQ[12] M_B_DQ13 E5 SB_DQ[13] M_B_DQ14 E3 SB_DQ[14] M_B_DQ15 G4 SB_DQ[15] M_B_DQ16 G2 SB_DQ[16] M_B_DQ17 G2 SB_DQ[17] M_B_DQ18 J6 SB_DQ[18] M_B_DQ19 J3 SB_DQ[19] M_B_DQ20 G1 SB_DQ[20] M_B_DQ21 G5 SB_DQ[21] M_B_DQ22 J2 SB_DQ[22] M_B_DQ23 J1 SB_DQ[23] M_B_DQ24 J5 SB_DQ[24] M_B_DQ25 L3 SB_DQ[25] M_B_DQ26 M1 SB_DQ[26] M_B_DQ27 M1 SB_DQ[27] M_B_DQ28 K4 SB_DQ[28] M_B_DQ29 M4 SB_DQ[29] M_B_DQ30 A3 SB_DQ[30] M_B_DQ31 N5 SB_DQ[31] M_B_DQ32 AE3 SB_DQ[32] M_B_DQ33 AG1 SB_DQ[33] M_B_DQ34 A3 SB_DQ[34] M_B_DQ35 AK1 SB_DQ[35] M_B_DQ36 AG4 SB_DQ[36] M_B_DQ37 AS3 SB_DQ[37] M_B_DQ38 AJ4 SB_DQ[38] M_B_DQ39 AH4 SB_DQ[39] M_B_DQ40 AK3 SB_DQ[40] M_B_DQ41 AK4 SB_DQ[41] M_B_DQ42 AM6 SB_DQ[42] M_B_DQ43 AN2 SB_DQ[43] M_B_DQ44 AK5 SB_DQ[44] M_B_DQ45 AK2 SB_DQ[45] M_B_DQ46 AM4 SB_DQ[46] M_B_DQ47 AM3 SB_DQ[47] M_B_DQ48 AP3 SB_DQ[48] M_B_DQ49 AN5 SB_DQ[49] M_B_DQ50 AN6 SB_DQ[50] M_B_DQ51 AN6 SB_DQ[51] M_B_DQ52 AN4 SB_DQ[52] M_B_DQ53 AN3 SB_DQ[53] M_B_DQ54 AT2 SB_DQ[54] M_B_DQ55 AT6 SB_DQ[55] M_B_DQ56 AN7 SB_DQ[56] M_B_DQ57 AP6 SB_DQ[57] M_B_DQ58 AP8 SB_DQ[58] M_B_DQ59 AT9 SB_DQ[59] M_B_DQ60 AT7 SB_DQ[60] M_B_DQ61 AP9 SB_DQ[61] M_B_DQ62 AR10 SB_DQ[62] M_B_DQ63 AR10 SB_DQ[63]

DDR SYSTEM MEMORY - B

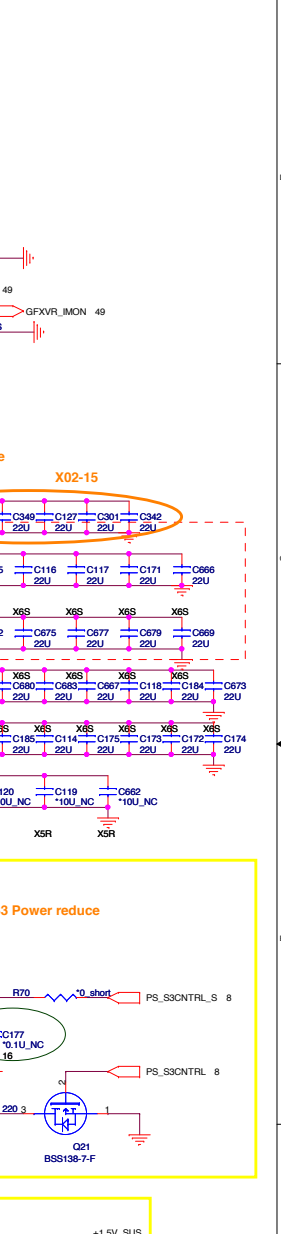
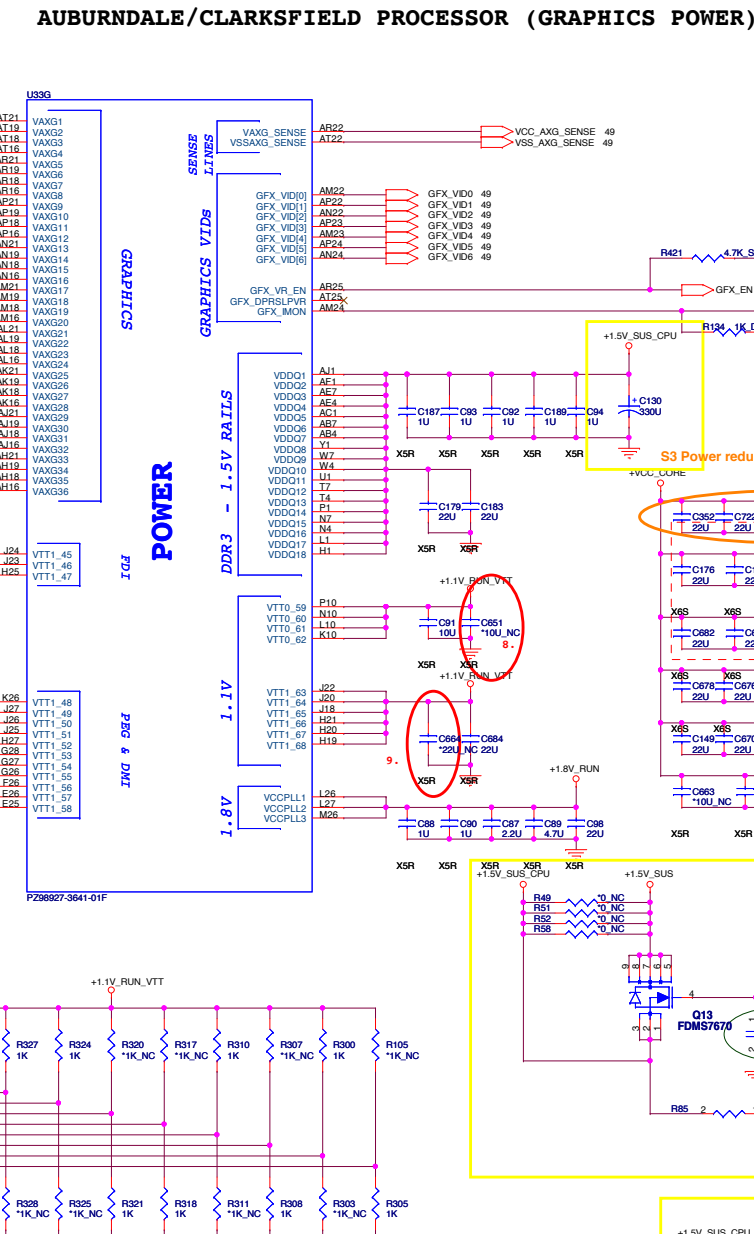
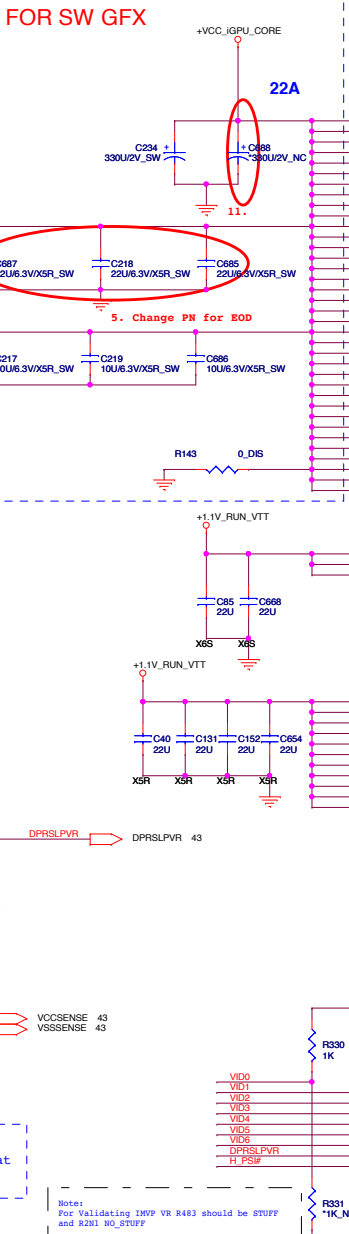
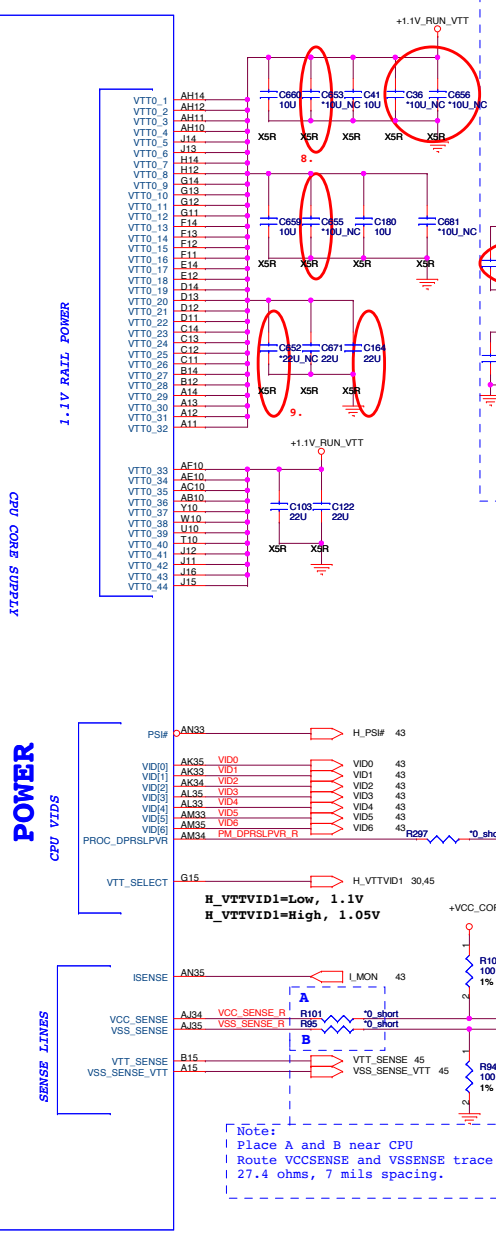
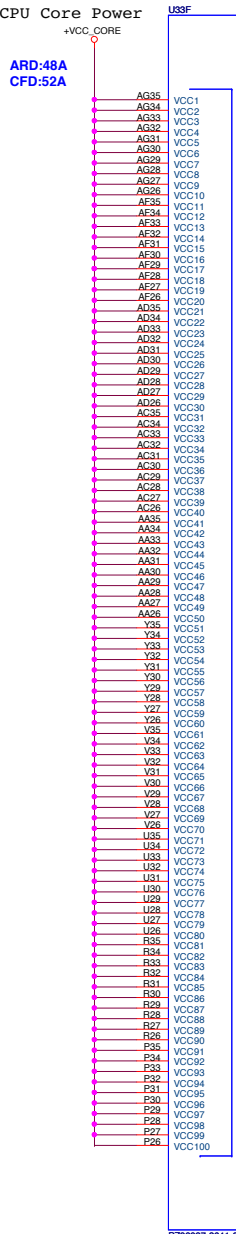
SB_CK[0] W8 M_B_CLK0 17 SB_CK[0] W9 M_B_CLK0# 17 SB_CK[0] M3 M_B_CKE0 17 SB_CK[1] V7 M_B_CLK1 17 SB_CK[1] V6 M_B_CLK1# 17 SB_CK[1] M2 M_B_CKE1 17 SB_CS#0 AB8 M_B_CS#0 17 SB_CS#1 AD6 M_B_CS#1 17 SB_ODT[0] AC7 M_B_ODT0 17 SB_ODT[1] AD1 M_B_ODT1 17 SB_DM[0] D4 M_B_DM0 M_B_DM[7:0] 17 SB_DM[1] E1 M_B_DM1 SB_DM[2] H3 M_B_DM2 SB_DM[3] K1 M_B_DM3 SB_DM[4] AL1 M_B_DM4 SB_DM[5] AL2 M_B_DM5 SB_DM[6] AR4 M_B_DM6 SB_DM[7] AR8 M_B_DM7 M_B_DQS#0 D5 M_B_DQS#0 M_B_DQS#7:0] 17 M_B_DQS#1 F4 M_B_DQS#1 M_B_DQS#2 J4 M_B_DQS#2 M_B_DQS#3 L4 M_B_DQS#3 M_B_DQS#4 AH2 M_B_DQS#4 M_B_DQS#5 AL4 M_B_DQS#5 M_B_DQS#6 AR5 M_B_DQS#6 M_B_DQS#7 AR8 M_B_DQS#7 M_B_DQS#0 C5 M_B_DQS#0 M_B_DQS#7:0] 17 M_B_DQS#1 E3 M_B_DQS#1 M_B_DQS#2 H4 M_B_DQS#2 M_B_DQS#3 M5 M_B_DQS#3 M_B_DQS#4 AS2 M_B_DQS#4 M_B_DQS#5 AL5 M_B_DQS#5 M_B_DQS#6 AP5 M_B_DQS#6 M_B_DQS#7 AR7 M_B_DQS#7 M_B_A[0] U5 M_B_A0 M_B_A[1] V2 M_B_A1 M_B_A[2] T5 M_B_A2 M_B_A[3] V3 M_B_A3 M_B_A[4] R1 M_B_A4 M_B_A[5] R2 M_B_A5 M_B_A[6] R2 M_B_A6 M_B_A[7] R6 M_B_A7 M_B_A[8] R4 M_B_A8 M_B_A[9] R5 M_B_A9 M_B_A[10] AB5 M_B_A10 M_B_A[11] P3 M_B_A11 M_B_A[12] R3 M_B_A12 M_B_A[13] AE7 M_B_A13 M_B_A[14] P5 M_B_A14 M_B_A[15] N1 M_B_A15

P298927-3641-01F



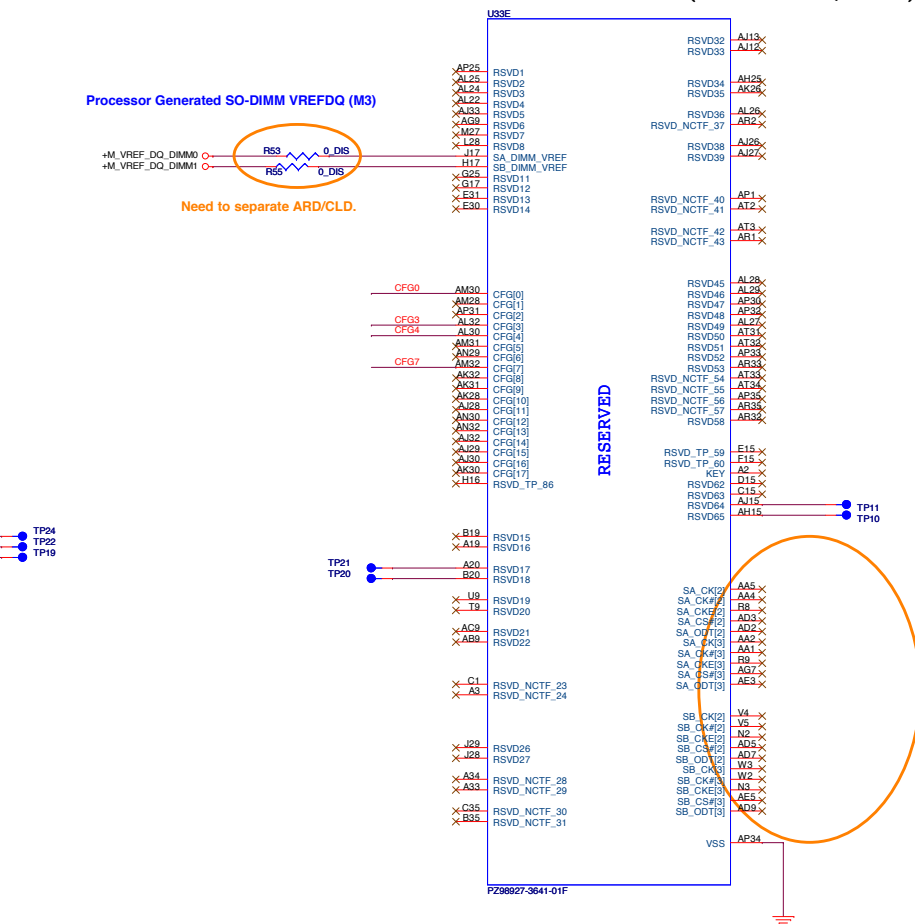
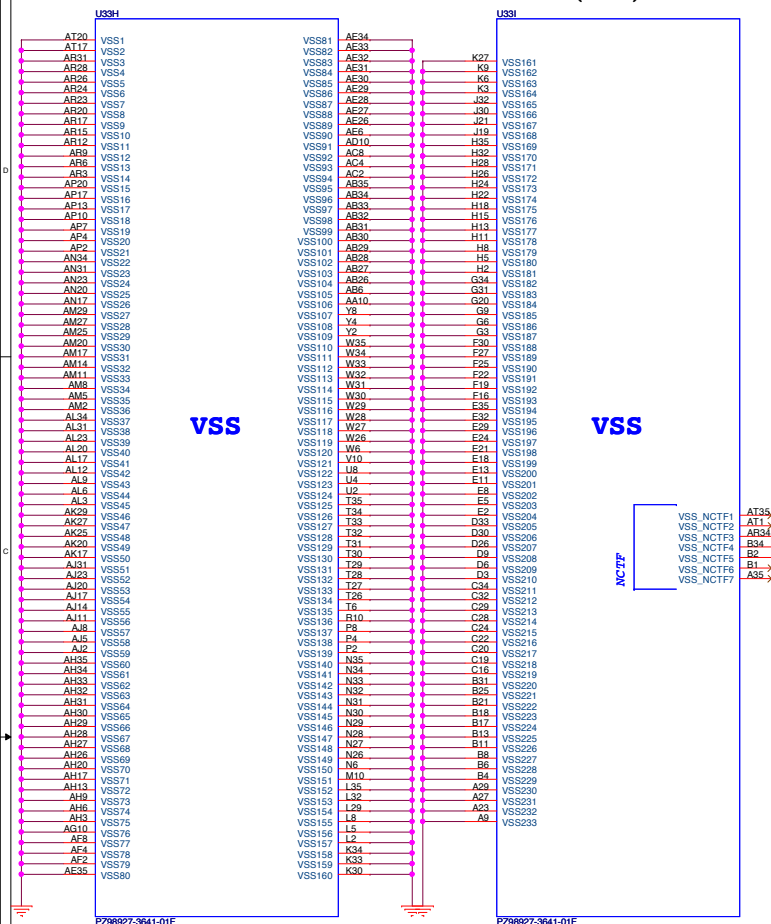
Quanta Computer Inc.
Project Name: GM7B

Title		CPU 24(DDR)	
Size	Document Number	GM7B_MB	Rev
			C3A
Date: Thursday, September 02, 2010		Sheet	5 of 54



AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

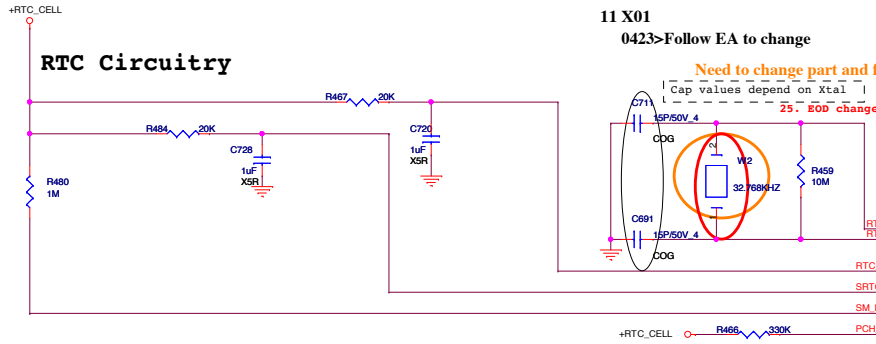


The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

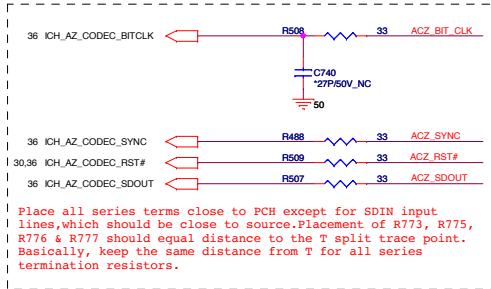


	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed
CFG7 (Clarkfield (only for early samples pre-ES))	Common motherboard design	For early samples pre-ES1 CFD

RTC Circuitry



IBEX PEAK-M (HDA, JTAG, SATA)

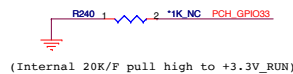


INTVRMEN - Integrated SUS 1.1V VRN Enable
High - Enable Internal VRs

0 ohm resistor within 0.5 inch of pin

Flash Descriptor Security Override

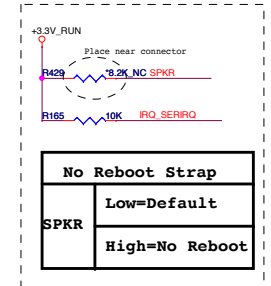
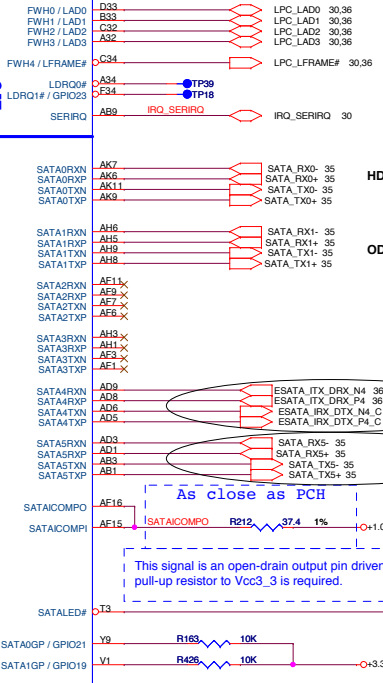
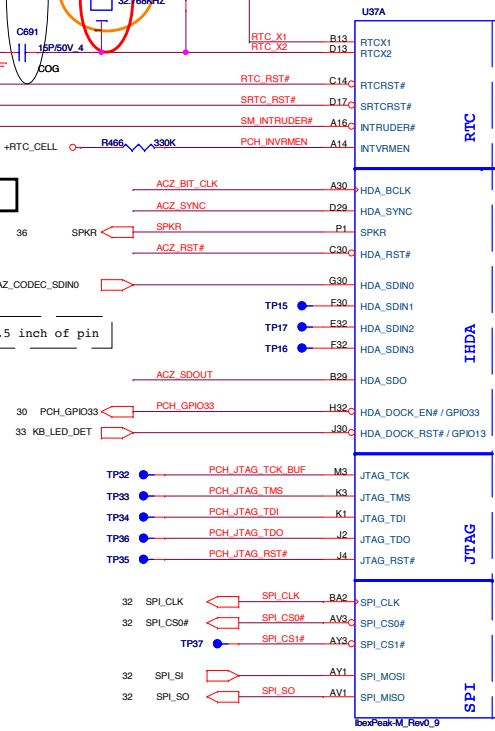
GPI033
Low = Enabled
High = Disabled



Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode. This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY.



Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

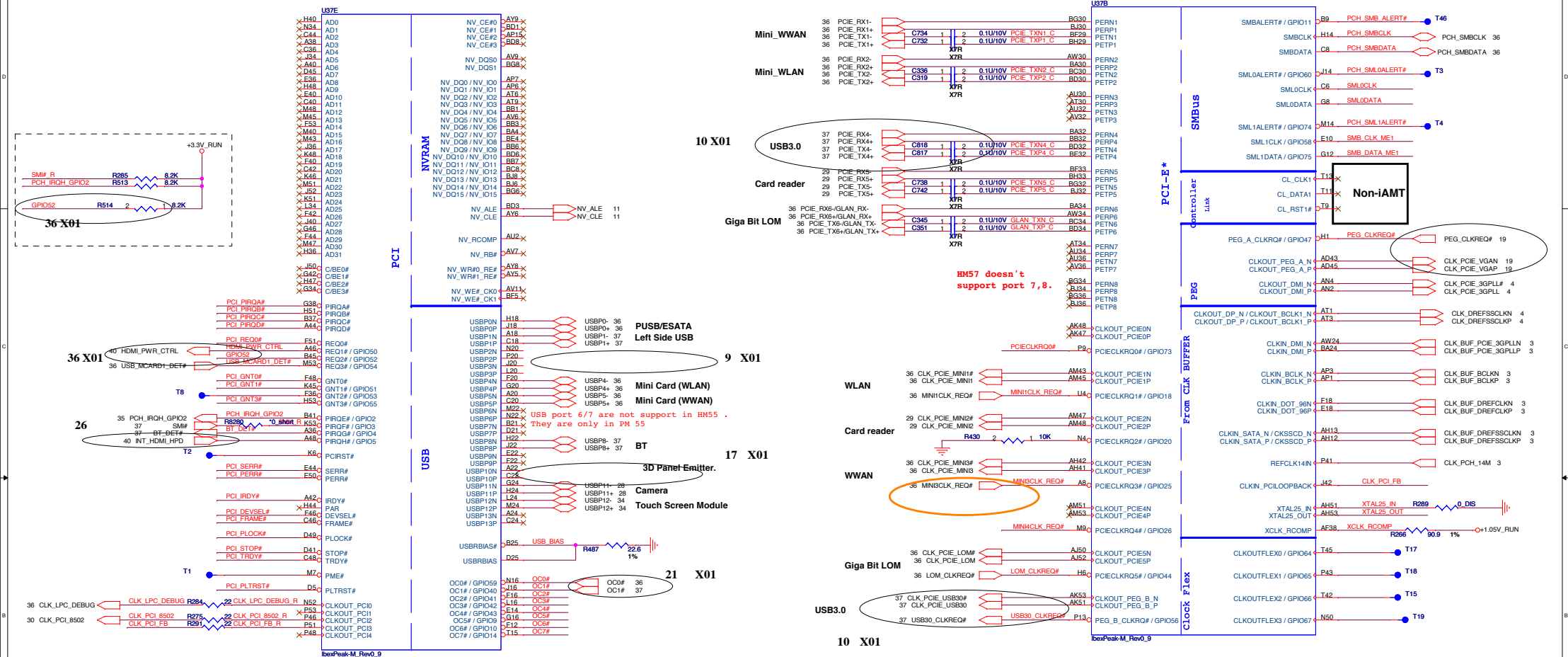


No Reboot Strap
Low=Default
High=No Reboot

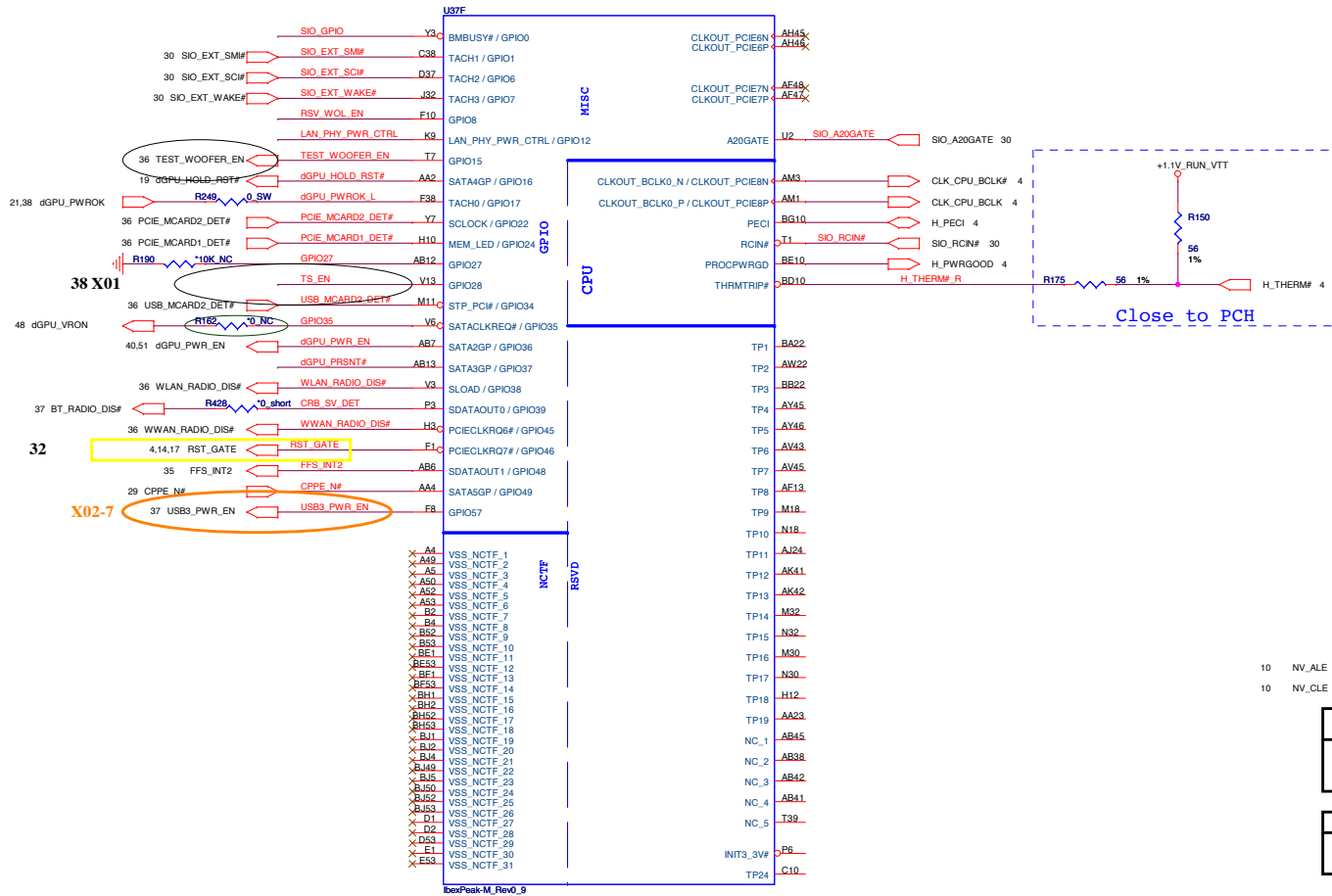
5 X01
0410>Reverse eSATA TX/RX
7 X01
0413>Reverse SATA5 TX+/-

IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

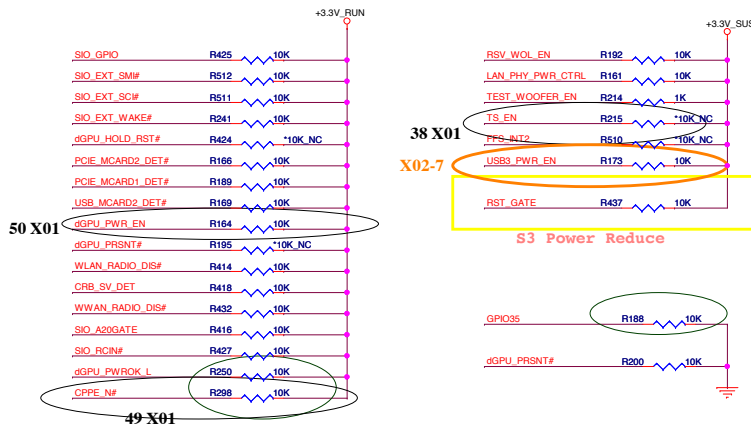


IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

Danbury Technology Enabled	
NV_ALE	High = Enable(Default) Low = Disable



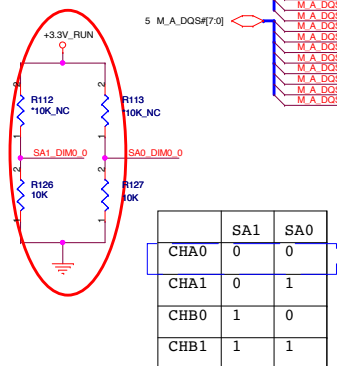
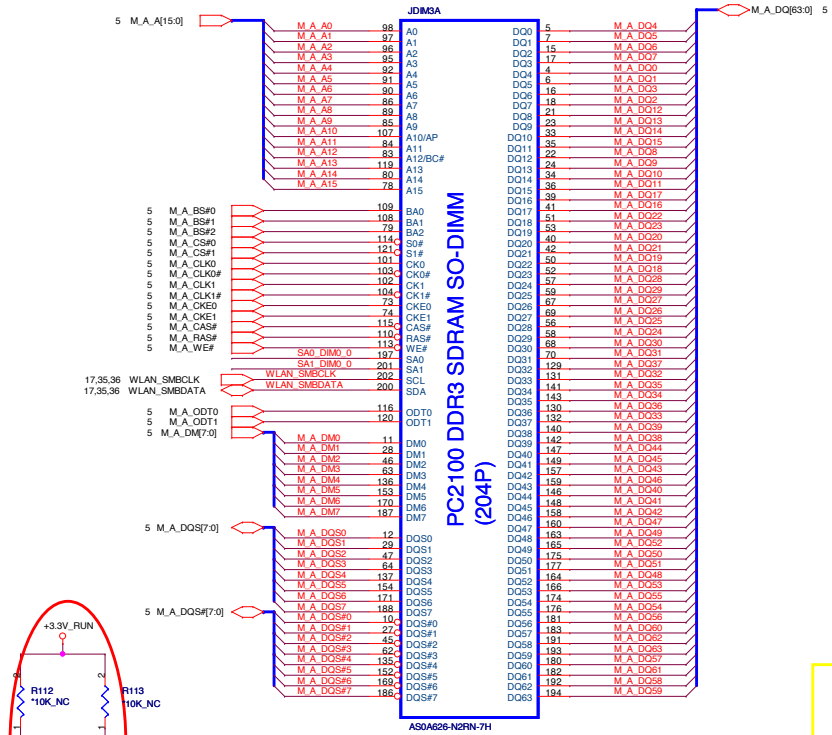
IBEX PEAK-M (GND)

U37H		
AB16	VSS[0]	
AA19	VSS[1]	VSS[80]
AA20	VSS[2]	VSS[81]
AA22	VSS[3]	VSS[82]
AM19	VSS[4]	VSS[83]
AA24	VSS[5]	VSS[84]
AA26	VSS[6]	VSS[85]
AA28	VSS[7]	VSS[86]
AA30	VSS[8]	VSS[87]
AA31	VSS[9]	VSS[88]
AA32	VSS[10]	VSS[89]
AB11	VSS[11]	VSS[90]
AB15	VSS[12]	VSS[91]
AB23	VSS[13]	VSS[92]
AB30	VSS[14]	VSS[93]
AB31	VSS[15]	VSS[94]
AB32	VSS[16]	VSS[95]
AB33	VSS[17]	VSS[96]
AB43	VSS[18]	VSS[97]
AB47	VSS[19]	VSS[98]
AB5	VSS[20]	VSS[99]
AB8	VSS[21]	VSS[100]
AC2	VSS[22]	VSS[101]
AC52	VSS[23]	VSS[102]
AD11	VSS[24]	VSS[103]
AD12	VSS[25]	VSS[104]
AD16	VSS[26]	VSS[105]
AD23	VSS[27]	VSS[106]
AD30	VSS[28]	VSS[107]
AD31	VSS[29]	VSS[108]
AD32	VSS[30]	VSS[109]
AD34	VSS[31]	VSS[110]
AU22	VSS[32]	VSS[111]
AD42	VSS[33]	VSS[112]
AD46	VSS[34]	VSS[113]
AD49	VSS[35]	VSS[114]
AD7	VSS[36]	VSS[115]
AE2	VSS[37]	VSS[116]
AE4	VSS[38]	VSS[117]
AF12	VSS[39]	VSS[118]
Y13	VSS[40]	VSS[119]
AH49	VSS[41]	VSS[120]
AI44	VSS[42]	VSS[121]
AF35	VSS[43]	VSS[122]
AP13	VSS[44]	VSS[123]
AN34	VSS[45]	VSS[124]
AF45	VSS[46]	VSS[125]
AF46	VSS[47]	VSS[126]
AF49	VSS[48]	VSS[127]
AF5	VSS[49]	VSS[128]
AF8	VSS[50]	VSS[129]
AG2	VSS[51]	VSS[130]
AG52	VSS[52]	VSS[131]
AH11	VSS[53]	VSS[132]
AH15	VSS[54]	VSS[133]
AH16	VSS[55]	VSS[134]
AH24	VSS[56]	VSS[135]
AH32	VSS[57]	VSS[136]
AV18	VSS[58]	VSS[137]
AH43	VSS[59]	VSS[138]
AH47	VSS[60]	VSS[139]
AH7	VSS[61]	VSS[140]
AI19	VSS[62]	VSS[141]
AJ2	VSS[63]	VSS[142]
AJ20	VSS[64]	VSS[143]
AJ22	VSS[65]	VSS[144]
AJ23	VSS[66]	VSS[145]
AJ26	VSS[67]	VSS[146]
AJ28	VSS[68]	VSS[147]
AJ32	VSS[69]	VSS[148]
AJ34	VSS[70]	VSS[149]
AT5	VSS[71]	VSS[150]
AJ4	VSS[72]	VSS[151]
AK12	VSS[73]	VSS[152]
AM41	VSS[74]	VSS[153]
AN19	VSS[75]	VSS[154]
AK26	VSS[76]	VSS[155]
AK22	VSS[77]	VSS[156]
AK23	VSS[78]	VSS[157]
AK28	VSS[79]	VSS[158]

ibexPeak-M_Rev0_9

U37I		
AV7	VSS[159]	VSS[259]
B11	VSS[160]	VSS[260]
B15	VSS[161]	VSS[261]
B19	VSS[162]	VSS[262]
B23	VSS[163]	VSS[263]
B31	VSS[164]	VSS[264]
B35	VSS[165]	VSS[265]
B39	VSS[166]	VSS[266]
B43	VSS[167]	VSS[267]
B47	VSS[168]	VSS[268]
B7	VSS[169]	VSS[269]
BG12	VSS[170]	VSS[270]
BB12	VSS[171]	VSS[271]
BB16	VSS[172]	VSS[272]
BB20	VSS[173]	VSS[273]
BB24	VSS[174]	VSS[274]
BB30	VSS[175]	VSS[275]
BB34	VSS[176]	VSS[276]
BB38	VSS[177]	VSS[277]
BB42	VSS[178]	VSS[278]
BB49	VSS[179]	VSS[279]
BC8	VSS[180]	VSS[280]
BC10	VSS[181]	VSS[281]
BC14	VSS[182]	VSS[282]
BC18	VSS[183]	VSS[283]
BC2	VSS[184]	VSS[284]
BC22	VSS[185]	VSS[285]
BC32	VSS[186]	VSS[286]
BC36	VSS[187]	VSS[287]
BC40	VSS[188]	VSS[288]
BC44	VSS[189]	VSS[289]
BC52	VSS[190]	VSS[290]
BD48	VSS[191]	VSS[291]
BD49	VSS[192]	VSS[292]
BD49	VSS[193]	VSS[293]
BD5	VSS[194]	VSS[294]
BE12	VSS[195]	VSS[295]
BE16	VSS[196]	VSS[296]
BE20	VSS[197]	VSS[297]
BE24	VSS[198]	VSS[298]
BE30	VSS[199]	VSS[299]
BE34	VSS[200]	VSS[300]
BE38	VSS[201]	VSS[301]
BE42	VSS[202]	VSS[302]
BE46	VSS[203]	VSS[303]
BE48	VSS[204]	VSS[304]
BE50	VSS[205]	VSS[305]
BE6	VSS[206]	VSS[306]
BE9	VSS[207]	VSS[307]
BF3	VSS[208]	VSS[308]
BF49	VSS[209]	VSS[309]
BF51	VSS[210]	VSS[310]
BG10	VSS[211]	VSS[311]
BG24	VSS[212]	VSS[312]
BG4	VSS[213]	VSS[313]
BG50	VSS[214]	VSS[314]
BH11	VSS[215]	VSS[315]
BH15	VSS[216]	VSS[316]
BH19	VSS[217]	VSS[317]
BH23	VSS[218]	VSS[318]
BH31	VSS[219]	VSS[319]
BH35	VSS[220]	VSS[320]
BH39	VSS[221]	VSS[321]
BH43	VSS[222]	VSS[322]
BH47	VSS[223]	VSS[323]
BH7	VSS[224]	VSS[324]
C12	VSS[225]	VSS[325]
C50	VSS[226]	VSS[326]
D51	VSS[227]	VSS[327]
E12	VSS[228]	VSS[328]
E16	VSS[229]	VSS[329]
E20	VSS[230]	VSS[330]
E24	VSS[231]	VSS[331]
E30	VSS[232]	VSS[332]
E34	VSS[233]	VSS[333]
E38	VSS[234]	VSS[334]
E42	VSS[235]	VSS[335]
E46	VSS[236]	VSS[336]
E48	VSS[237]	VSS[337]
E6	VSS[238]	VSS[338]
E8	VSS[239]	VSS[339]
FA9	VSS[240]	VSS[340]
F5	VSS[241]	VSS[341]
G10	VSS[242]	VSS[342]
G14	VSS[243]	VSS[343]
G18	VSS[244]	VSS[344]
G2	VSS[245]	VSS[345]
G22	VSS[246]	VSS[346]
G32	VSS[247]	VSS[347]
G36	VSS[248]	VSS[348]
G40	VSS[249]	VSS[349]
G44	VSS[250]	VSS[350]
G52	VSS[251]	VSS[351]
AF39	VSS[252]	VSS[352]
H16	VSS[253]	VSS[353]
H20	VSS[254]	VSS[354]
H30	VSS[255]	VSS[355]
H34	VSS[256]	VSS[356]
H38	VSS[257]	VSS[357]
H42	VSS[258]	VSS[358]

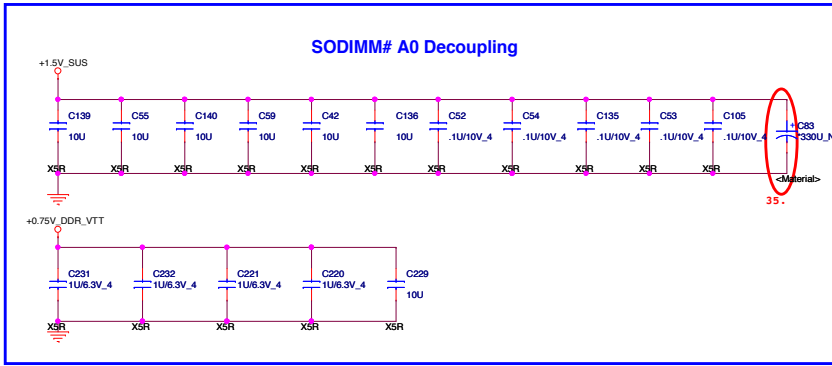
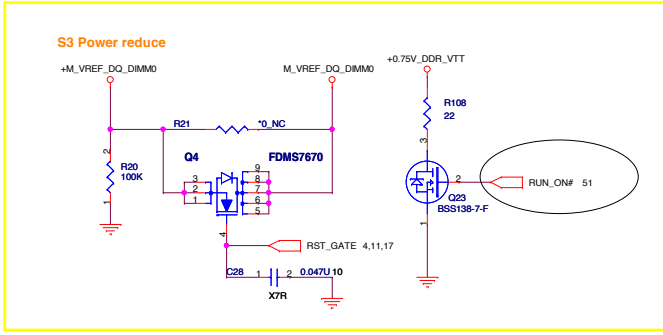
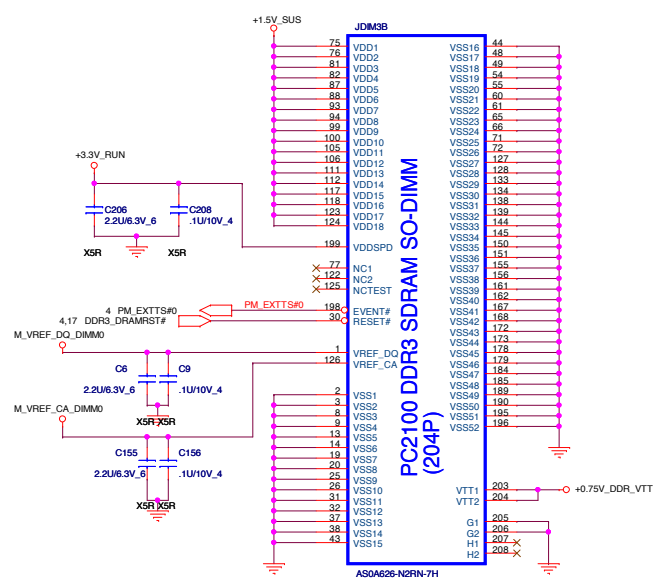
ibexPeak-M_Rev0_9



Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

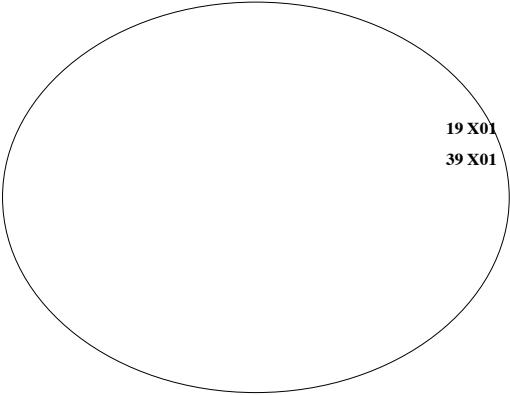
Need to check again

CHA_DIMM0_HEIGHT




Remove JDIMM4 to fix co-layout

8 X01
0413>Add _DIS for SODIMM

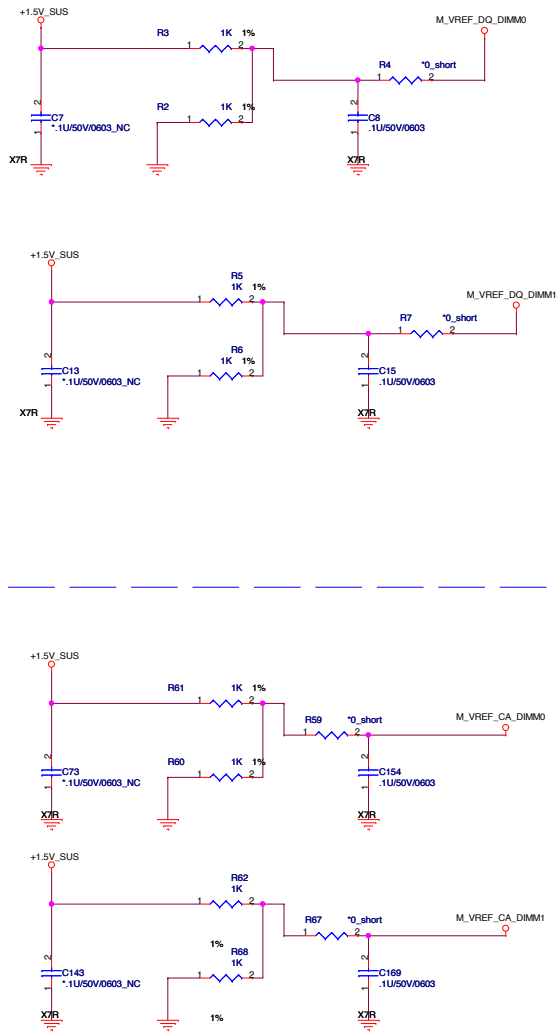


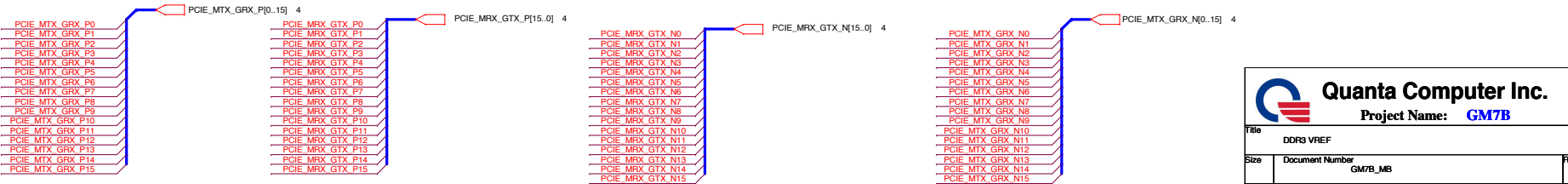
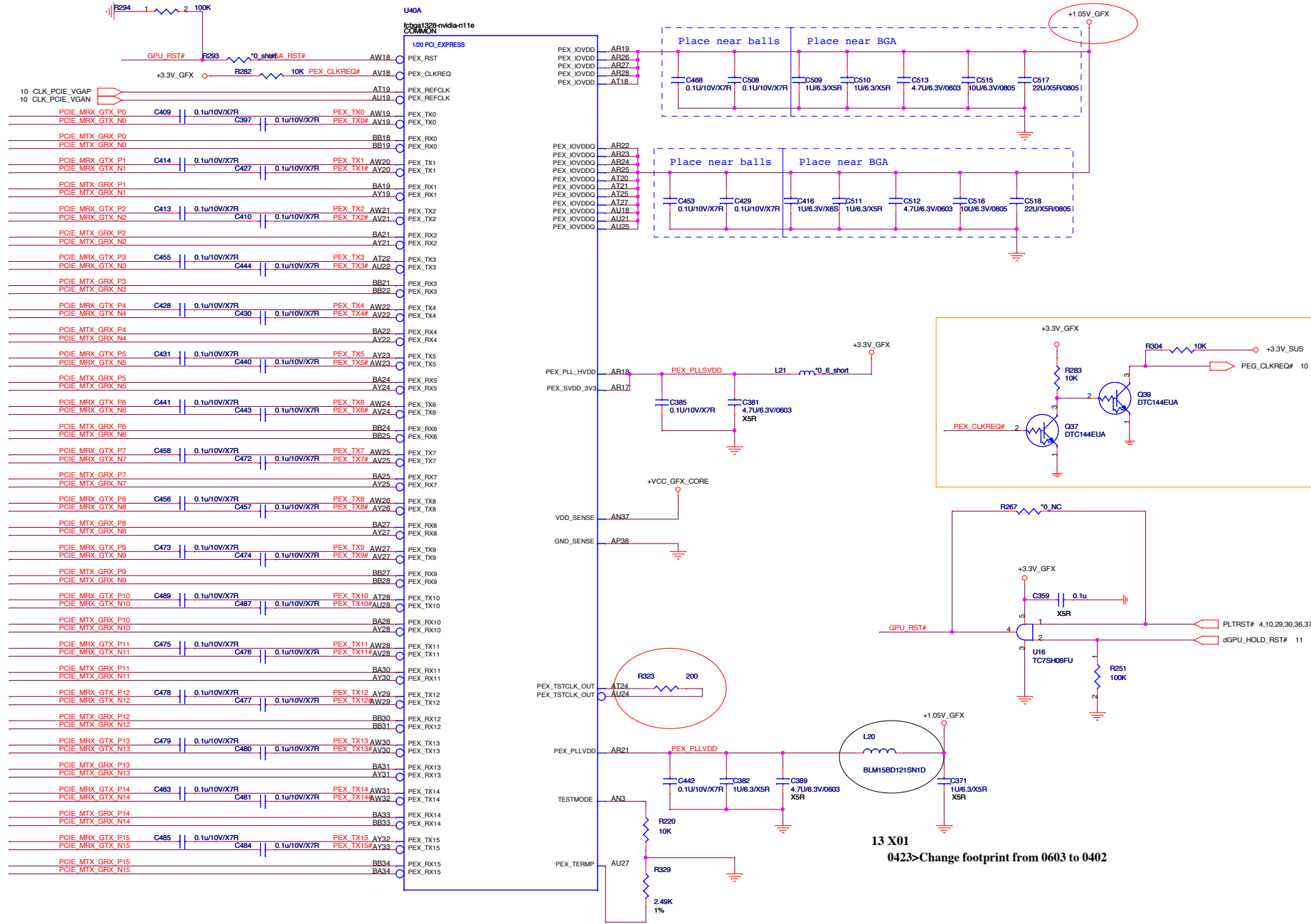
19 X01
39 X01

Remove JDIMM4 to fix co-layout

		Quanta Computer Inc.	
		Project Name: GM7B	
Title: BLOCK			
Size	Document Number		Rev
	GM7B_MB		C3A
Date: Thursday, September 02, 2010			
		Sheet	16 of 54

Fixed SO-DIMM VREF_DQ (M1): Default





27 FBC_D[63..0]
27 FBC_DOM[7..0]
27 FBC_DOSP[7..0]
27 FBC_DOSN[7..0]

U40D
ibpnt328-nvidia-n11e
COMMON

FBC_D0 M6
FBC_D1 M4
FBC_D2 M7
FBC_D3 M5
FBC_D4 K5
FBC_D5 K6
FBC_D6 L7
FBC_D7 K7
FBC_D8 P4
FBC_D9 B8
FBC_D10 R4
FBC_D11 R5
FBC_D12 T5
FBC_D13 T4
FBC_D14 U4
FBC_D15 T6
FBC_D16 U3
FBC_D17 T1
FBC_D18 V3
FBC_D19 T2
FBC_D20 R3
FBC_D21 P3
FBC_D22 N1
FBC_D23 N2
FBC_D24 J2
FBC_D25 K3
FBC_D26 J3
FBC_D27 J1
FBC_D28 M3
FBC_D29 M2
FBC_D30 M1
FBC_D31 M1
FBC_D32 F12
FBC_D33 D13
FBC_D34 G12
FBC_D35 E12
FBC_D36 E10
FBC_D37 E10
FBC_D38 G11
FBC_D39 G10
FBC_D40 D14
FBC_D41 F15
FBC_D42 D15
FBC_D43 E15
FBC_D44 E16
FBC_D45 D16
FBC_D46 D17
FBC_D47 F16
FBC_D48 C17
FBC_D49 A16
FBC_D50 C18
FBC_D51 B16
FBC_D52 C15
FBC_D53 C14
FBC_D54 A13
FBC_D55 B13
FBC_D56 B9
FBC_D57 C10
FBC_D58 C9
FBC_D59 A9
FBC_D60 C12
FBC_D61 B12
FBC_D62 C13
FBC_D63 A12

FBC_DOM0 K4
FBC_DOM1 R7
FBC_DOM2 T3
FBC_DOM3 L3
FBC_DOM4 D10
FBC_DOM5 G15
FBC_DOM6 C16
FBC_DOM7 C11

FBC_DOSP0 L4
FBC_DOSP1 U7
FBC_DOSP2 R1
FBC_DOSP3 K1
FBC_DOSP4 D11
FBC_DOSP5 G17
FBC_DOSP6 A15
FBC_DOSP7 B10

FBC_DOSN0 M4
FBC_DOSN1 T7
FBC_DOSN2 R2
FBC_DOSN3 K2
FBC_DOSN4 D12
FBC_DOSN5 G16
FBC_DOSN6 B15
FBC_DOSN7 A10

FBC_DOS_WP0
FBC_DOS_WP1
FBC_DOS_WP2
FBC_DOS_WP3
FBC_DOS_WP4
FBC_DOS_WP5
FBC_DOS_WP6
FBC_DOS_WP7

FBC_DOS_RN0
FBC_DOS_RN1
FBC_DOS_RN2
FBC_DOS_RN3
FBC_DOS_RN4
FBC_DOS_RN5
FBC_DOS_RN6
FBC_DOS_RN7

COMMAND BUS
REFERENCE

GND_REF
GND_REF

FBC_CMD0 H5
FBC_CMD1 G1N FBC_CMD1
FBC_CMD2 G5
FBC_CMD3 F4
FBC_CMD4 G2
FBC_CMD5 G1
FBC_CMD6 G1
FBC_CMD7 E1
FBC_CMD8 J5
FBC_CMD9 E3
FBC_CMD10 H6
FBC_CMD11 C2
FBC_CMD12 F3
FBC_CMD13 E2
FBC_CMD14 D1
FBC_CMD15 D2
FBC_CMD16 E8
FBC_CMD17 D2N FBC_CMD17
FBC_CMD18 E7
FBC_CMD19 D6
FBC_CMD20 B7
FBC_CMD21 A7
FBC_CMD22 C7
FBC_CMD23 A6
FBC_CMD24 E9
FBC_CMD25 C5
FBC_CMD26 F8
FBC_CMD27 B3
FBC_CMD28 C6
FBC_CMD29 B5
FBC_CMD30 A4
FBC_CMD31 B4

FBC_DEBUG0 J6
FBC_DEBUG1 F9

FBC_CLK0 H3
FBC_CLK0 H4
FBC_CLK1 C8
FBC_CLK1 D8

FBC_WCK01 P7
FBC_WCK01 N7
FBC_WCK23 N5
FBC_WCK23 K2
FBC_WCK45 G14
FBC_WCK45 G13
FBC_WCK87 E13
FBC_WCK87 F13

FBC_PLL_AVDD H8 FBA_PLLAVDD 20

C395
0.1U10V/X7R

Remove test pad for
VRAM power shape.

+1.5V_GFX

U40E
ibpnt328-nvidia-n11e
COMMON

FBVDDQ
A2 FBVDDQ
A3 FBVDDQ
A3B FBVDDQ
AB35 FBVDDQ
AC38 FBVDDQ
AD35 FBVDDQ
AD41 FBVDDQ
AE35 FBVDDQ
AE36 FBVDDQ
AG35 FBVDDQ
AG36 FBVDDQ
AK35 FBVDDQ
AL35 FBVDDQ
B1 FBVDDQ
B2 FBVDDQ
B29 FBVDDQ
B33 FBVDDQ
B6 FBVDDQ
C1 FBVDDQ
C4 FBVDDQ
D26 FBVDDQ
D3 FBVDDQ
D4 FBVDDQ
D5 FBVDDQ
D9 FBVDDQ
E32 FBVDDQ
E4 FBVDDQ
E8 FBVDDQ
E2 FBVDDQ
F5 FBVDDQ
F6 FBVDDQ
E7 FBVDDQ
G19 FBVDDQ
G30 FBVDDQ
G6 FBVDDQ
G8 FBVDDQ
G9 FBVDDQ
H10 FBVDDQ
H12 FBVDDQ
H13 FBVDDQ
H15 FBVDDQ
H16 FBVDDQ
H18 FBVDDQ
H19 FBVDDQ

FBVDDQ_PROBE V8

FB_CAL_PD_VDDQ V6

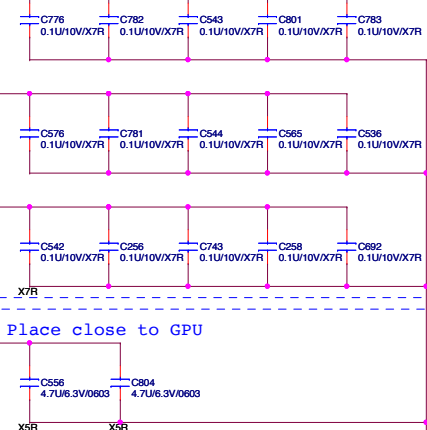
FB_CAL_PU_GND V7

FB_CALTERM_GND V4

+1.5V_GFX

GPU FBVDDQ Decoupling

Place close to GPU balls



Place close to GPU

X5R

X5R

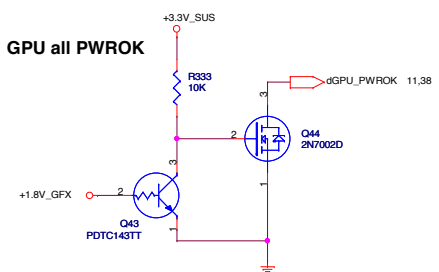
FBVDDQ_PROBE V8

FB_CAL_PD_VDDQ V6

FB_CAL_PU_GND V7

FB_CALTERM_GND V4

GPU all PWROK

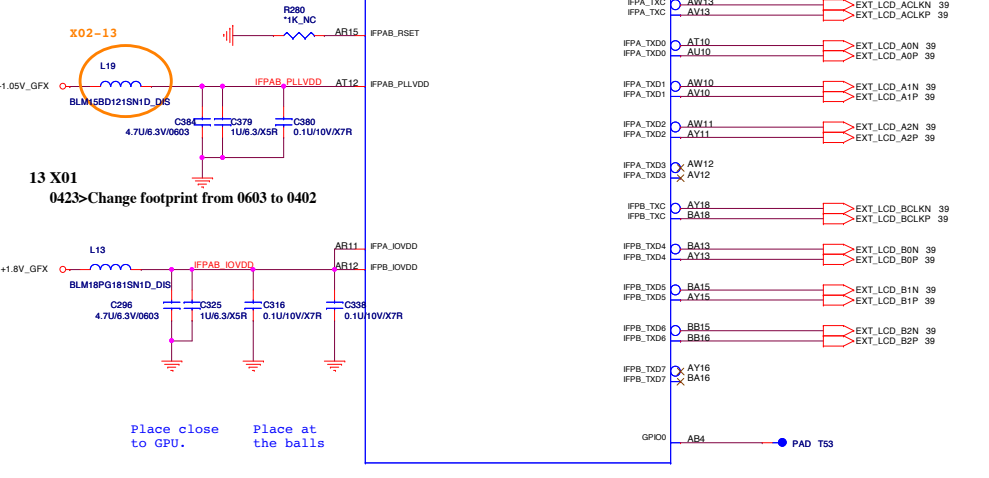


Quanta Computer Inc.

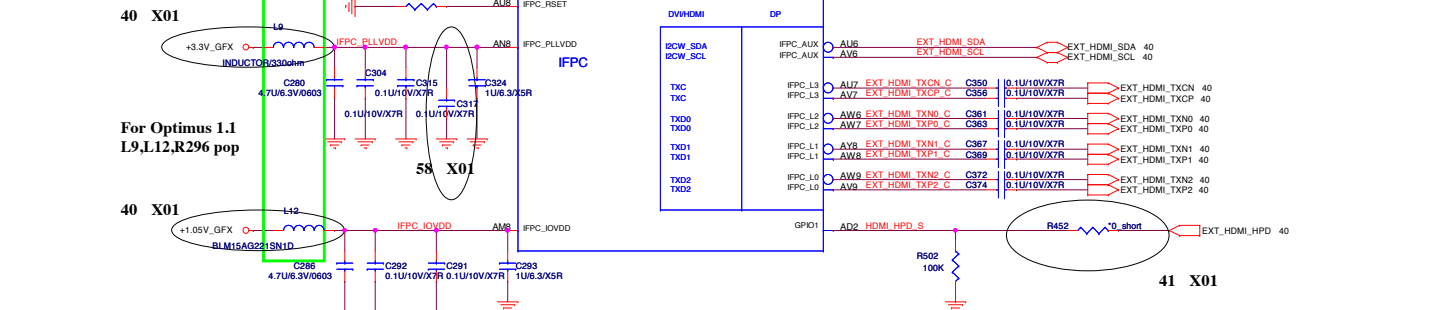
Project Name: GM7B

Title	DDR3 VREF		
Size	Document Number	GM7B_MB	Rev CGA
Date	Thursday, September 02, 2010	Sheet 21 of 54	

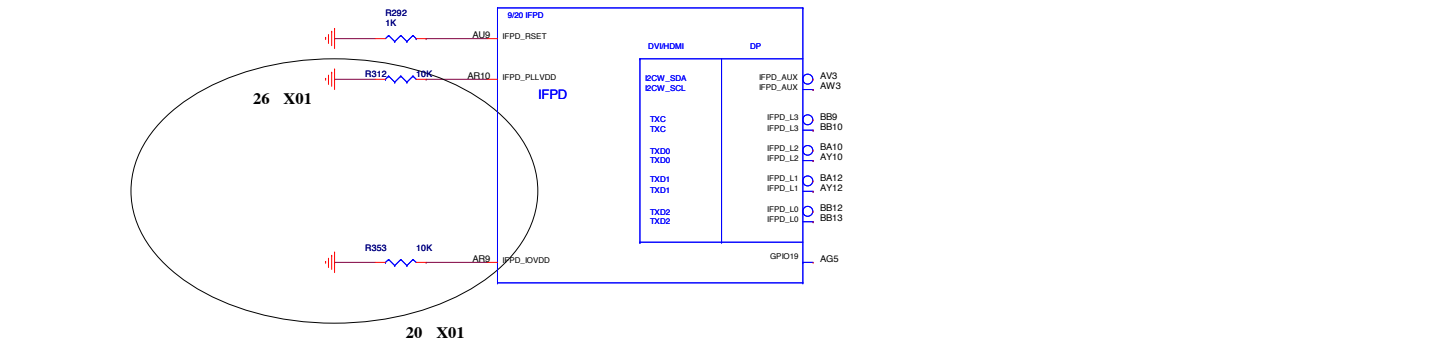
IFPA/B LVDS Dual Link



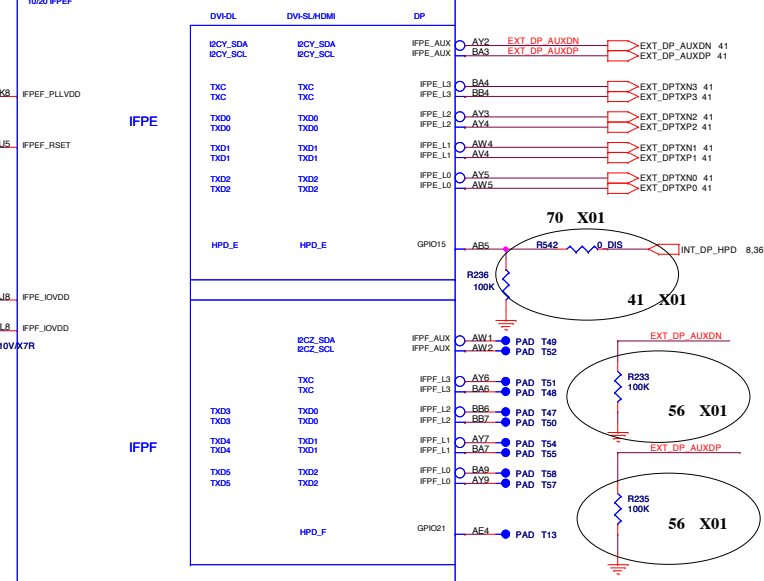
IFPC HDMI



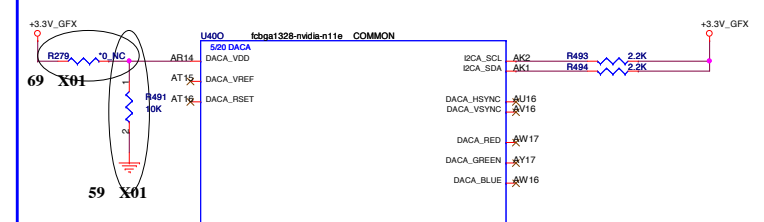
IFPD DP (eDP)



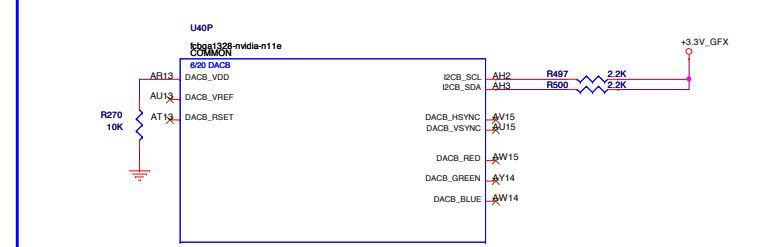
IFPE/F TMSD DVI-I



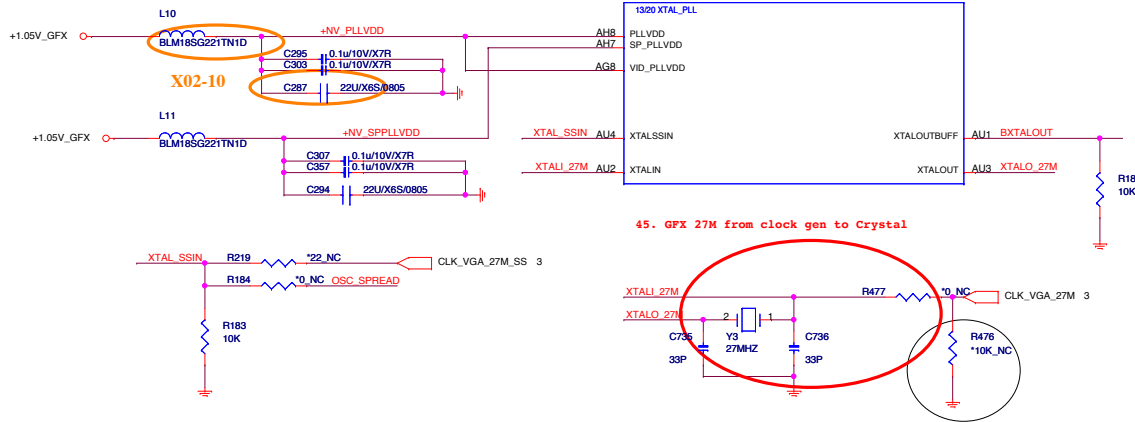
DAC_A VGA



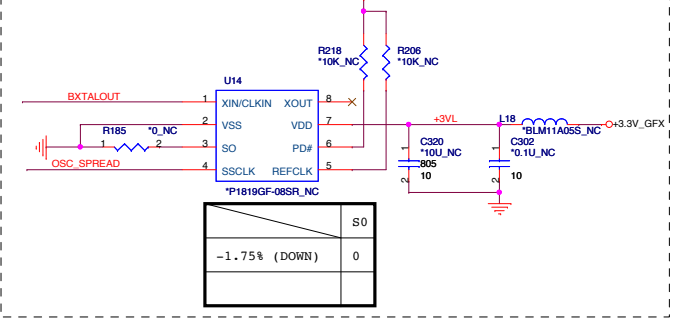
DAC_B Header



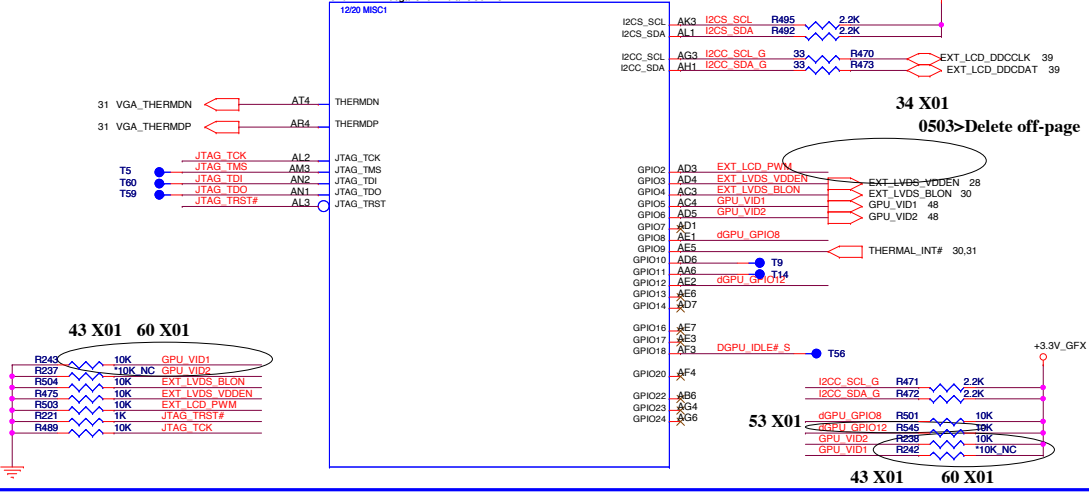
External SS



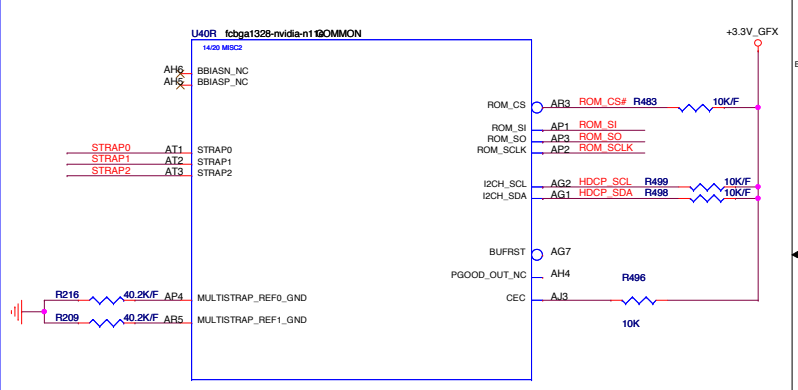
Spread Spectrum



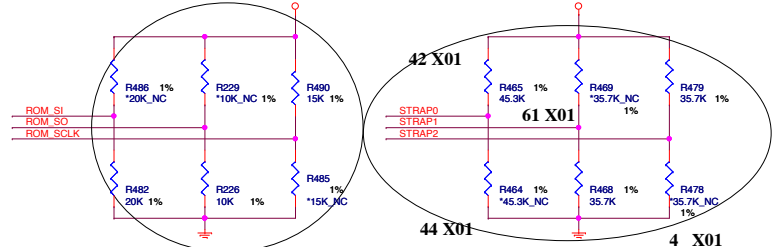
GPIOs, Thermal Sensor



BIOS ROM



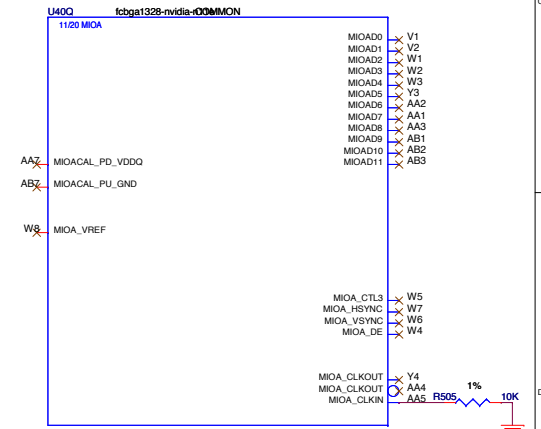
Straps



Strap Pin Mode Table	
Pin Name	Multi-Level Bit [3:0]
STRAP0	USER[3:0]
STRAP1	3GIO_PADCFG[3:0]
STRAP2	PCI_DEVID[3:0]
ROM_SCLK	PCI_DEVID[4] SUB_VENDOR SLOT_CLK PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3:0]
ROM_SO	XCLK 417 FB_0 BAR_SIZE SMB_ALT_ADDR VGA_DEVICE

Multi-Level Mode straps			
		PU	PD
N11E-GE	STRAP2		15K
	ROM_SCLK	15K	
N11P-GT-B	STRAP2		20K
	ROM_SCLK	15K	
Hynix 128Mx16	ROM_SI		35K
Hynix 64Mx16	ROM_SI		15K
Samsung 128Mx16	ROM_SI		45K
Samsung 64Mx16	ROM_SI		20K

NVGEM and MIOA



Strapping Resistor Value Decode

	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

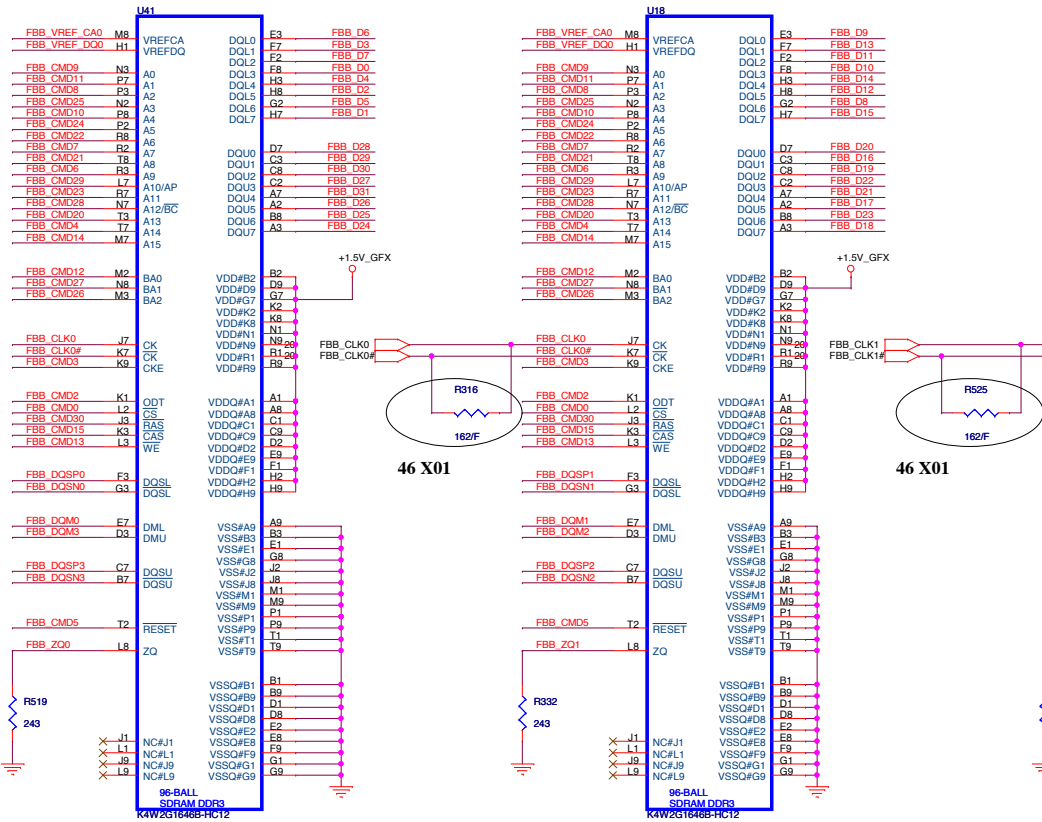
Config	Description	Decode	R482	R482 Part Number
31GM7MB0000	ARD+N11P-SAM (64x16) 1G	0011	20K	CS32002FB29
31GM7MB00020	ARD+N11P-HYN (64x16) 1G	0010	15K	CS31502FB24
31GM7MB00050	CLF+N11E-SAM (128x16) 3G	0111	45.3K	CS34532FB00
31GM7MB00070	CLF+N11E-HYN (128x16) 3G	0110	35.7K	CS33572FB13

Project Name: GM7B

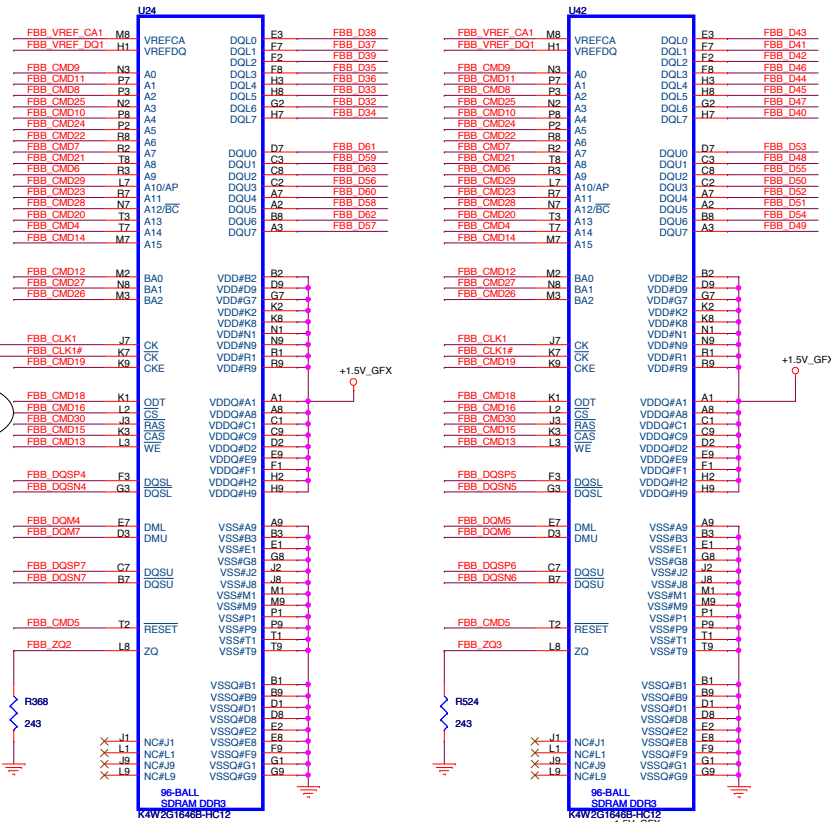
Title	DDR3 VREF		
Size	Document Number	GM7B_MB	Rev C5A
Date	Thursday, September 02, 2010	Sheet 23 of 54	

20 FBB_CMD[30..0]
20 FBB_D[63..0]
20 FBB_DQM[7..0]
20 FBB_DQSP[7..0]
20 FBB_DQSN[7..0]

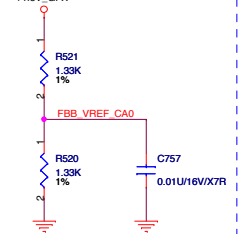
Memory Lower Partition B



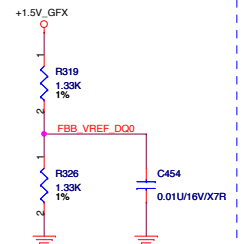
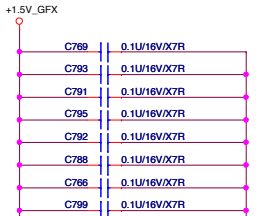
Memory Upper Partition B



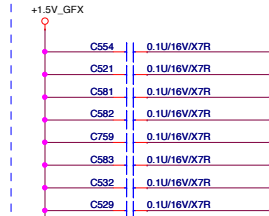
15V GFX



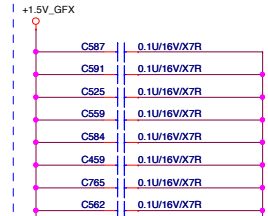
Decoupling for U1



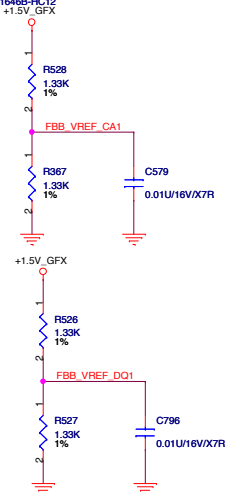
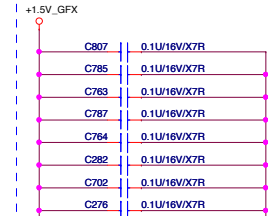
Decoupling for U2



Decoupling for U3

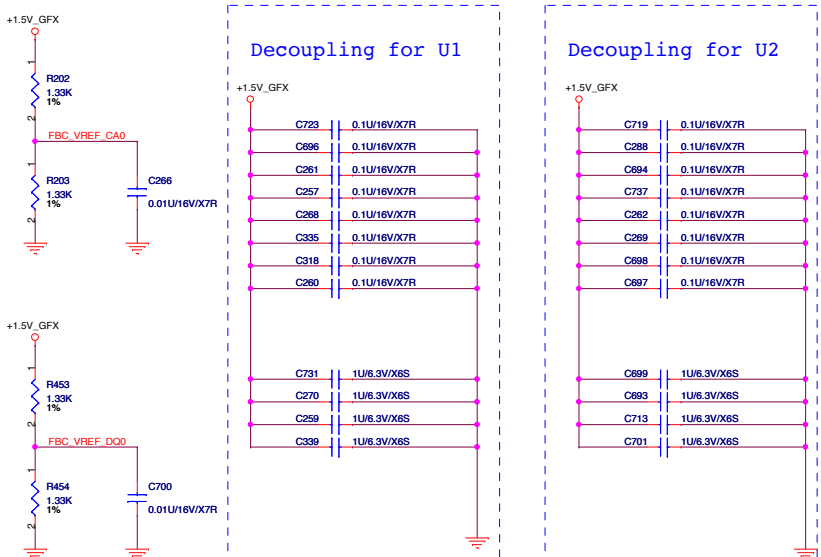
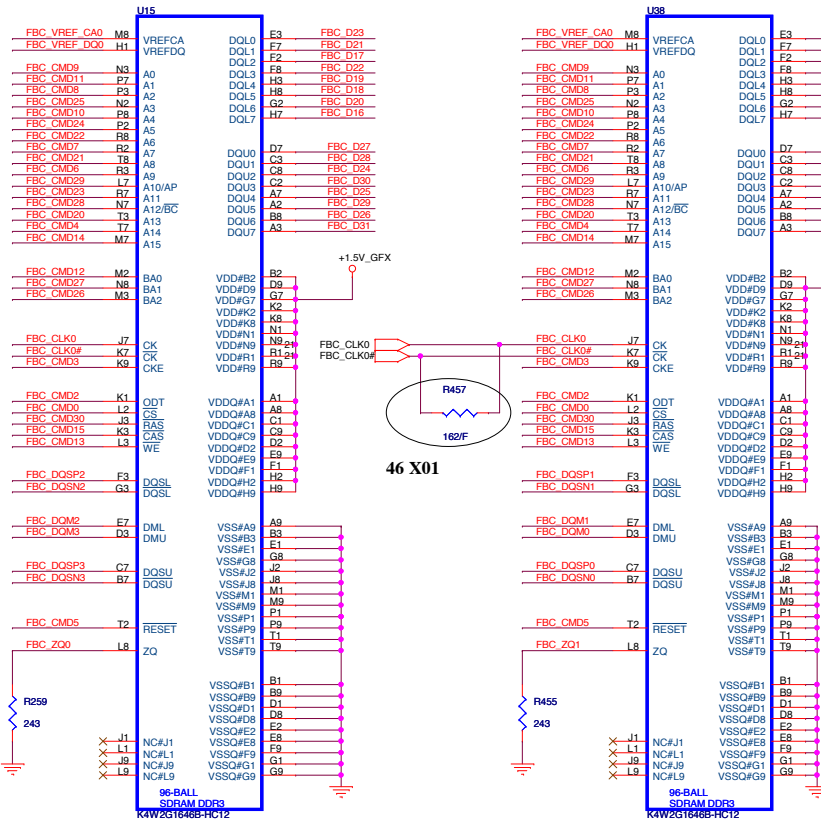


Decoupling for U4

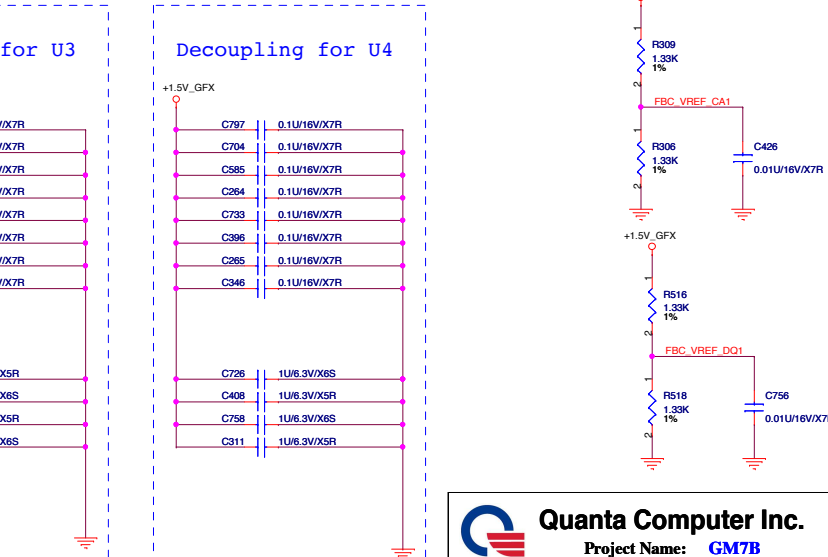
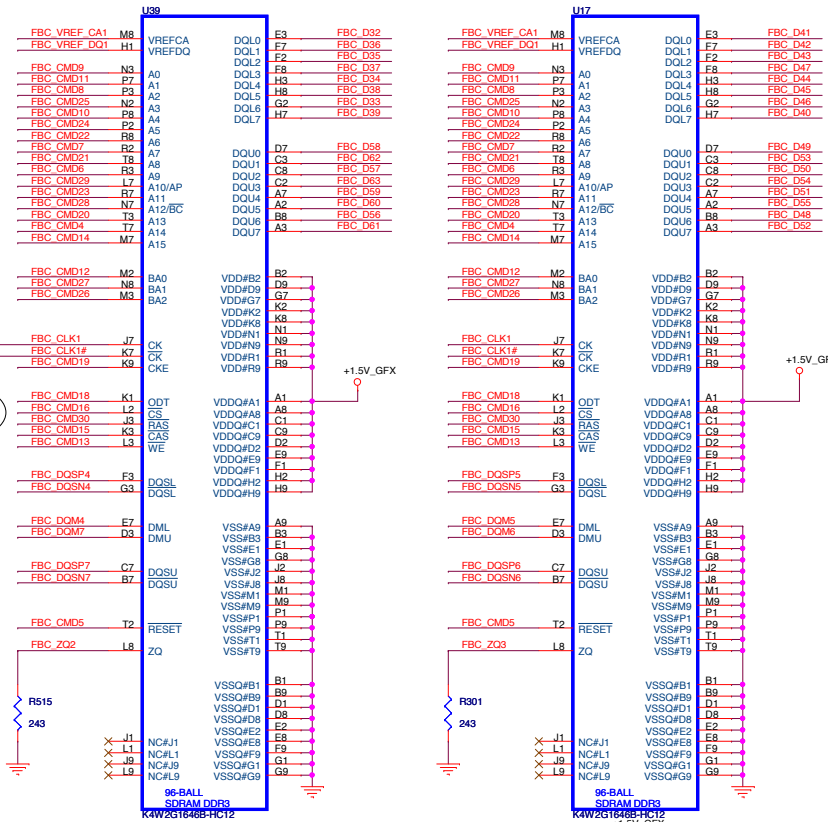


21 FBC_CMD[30..0]
21 FBC_D[63..0]
21 FBC_DQM[7..0]
21 FBC_DQSP[7..0]
21 FBC_DQSN[7..0]

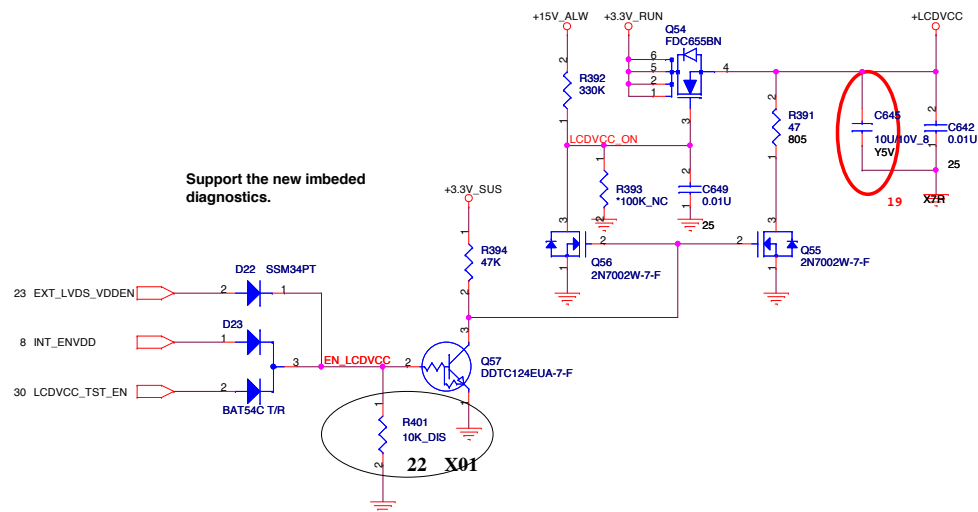
Memory Lower Partition C



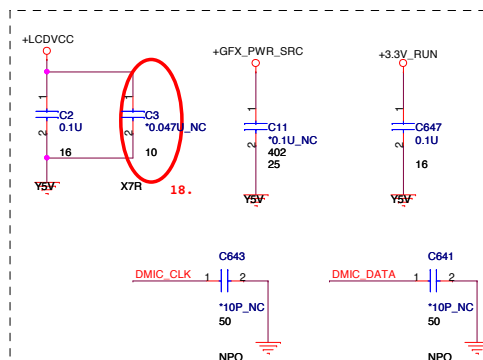
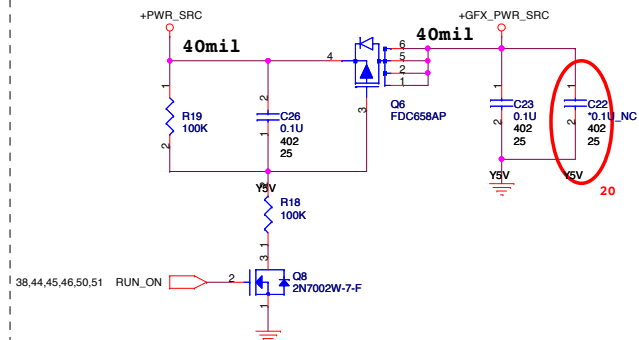
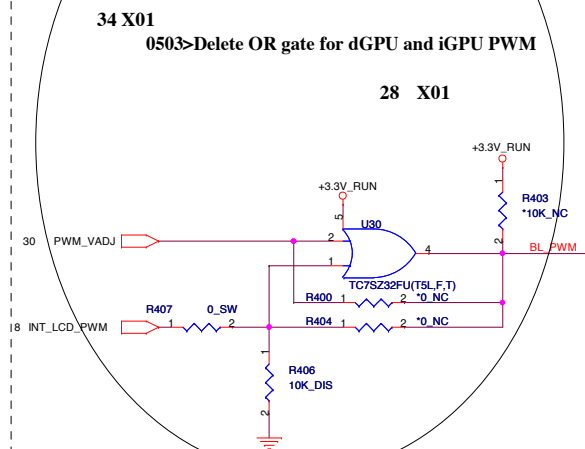
Memory Upper Partition C



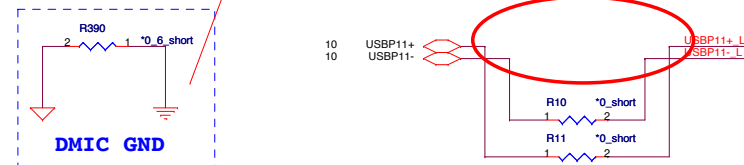
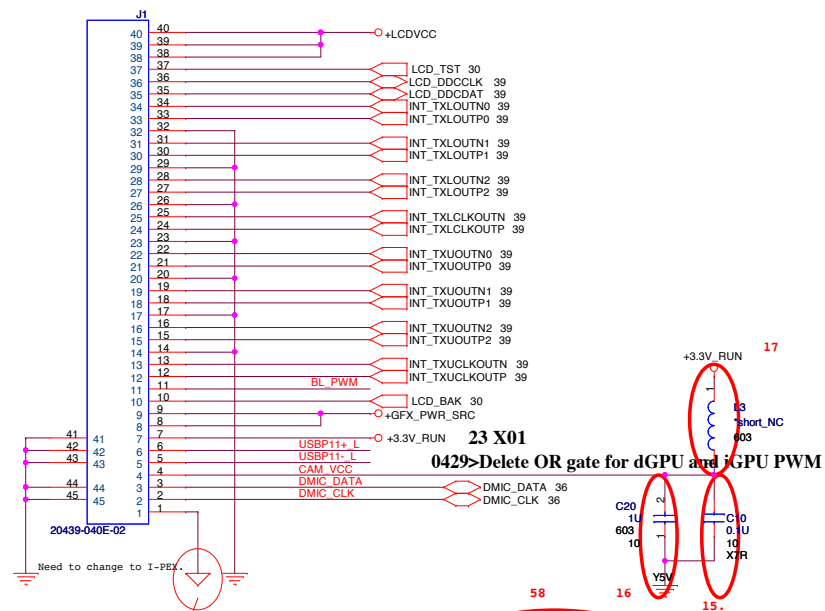
Panel VCC



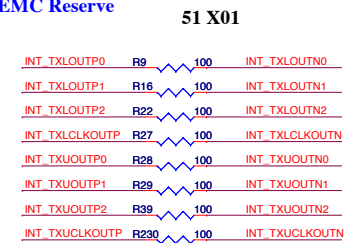
Backlight Control



40Pin LVDS & Array Microphone & Camera Connector



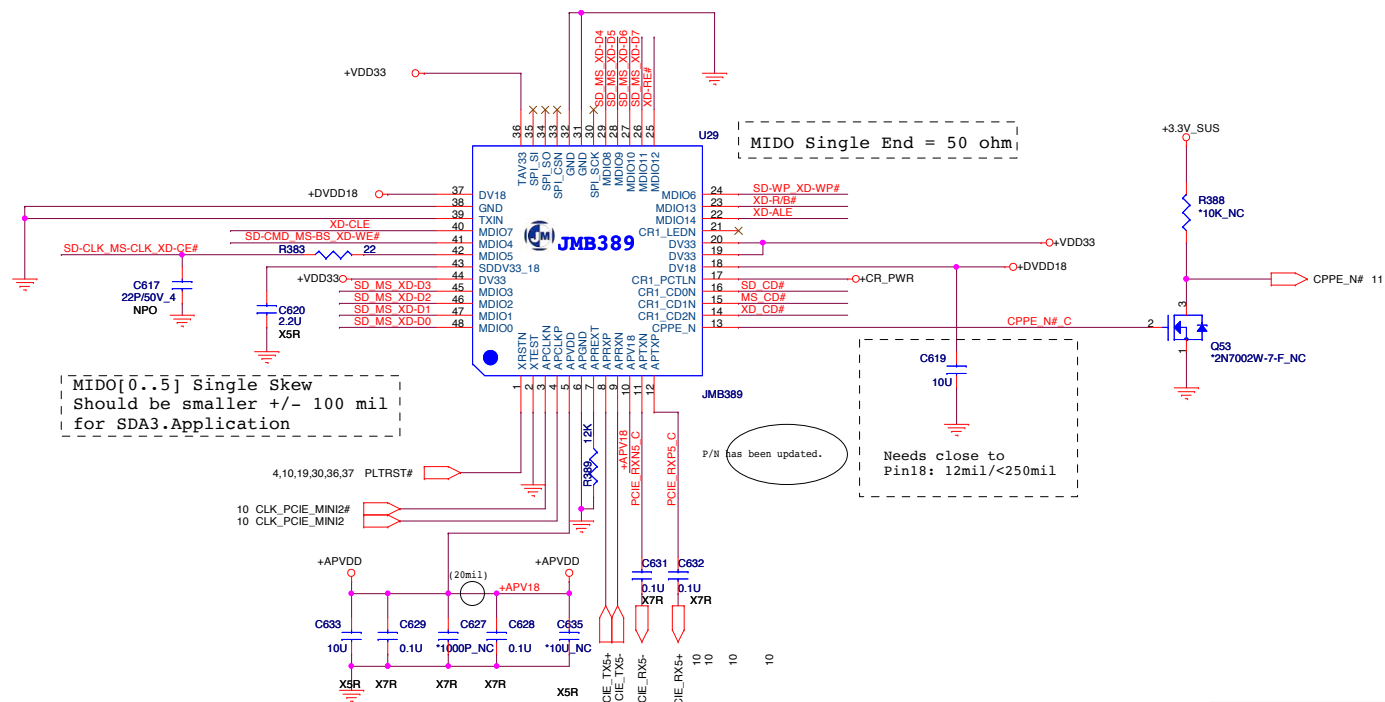
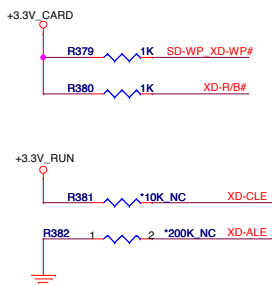
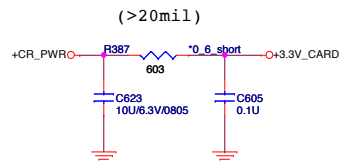
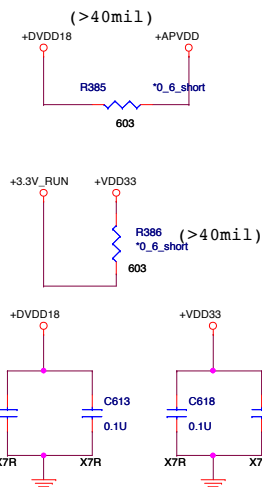
EMC Reserve

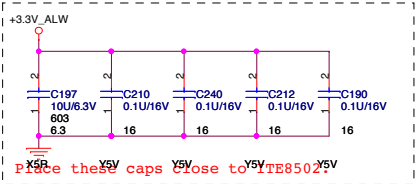
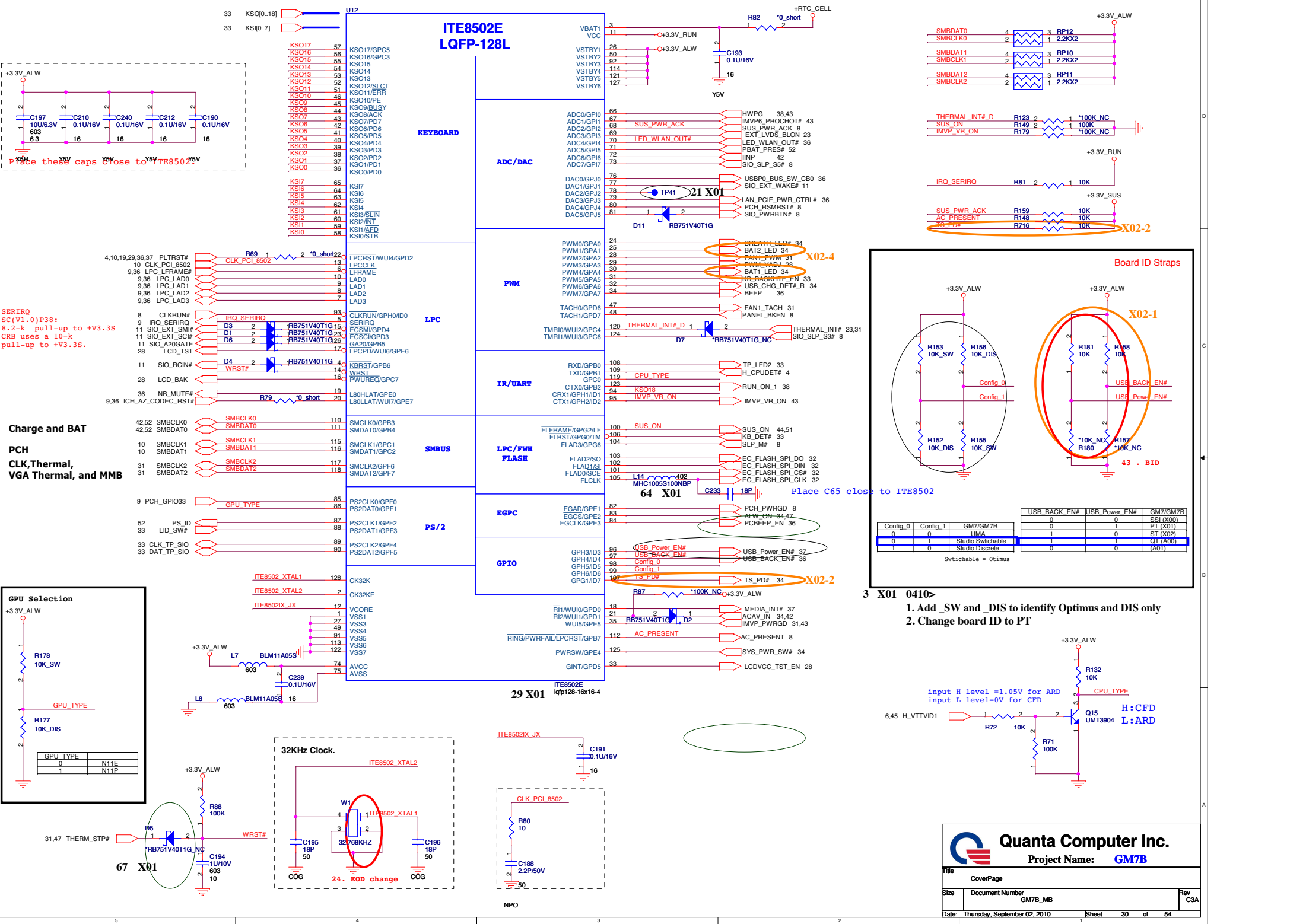


Please R close to pin of LCD connector, J1

17 X01

PTN	Default	SD	NMC	MS	XD
MDI000	SD/NMC/MS/xd	SD D0	MS D0	XD D0	
MDI001		SD D1	MS D1	XD D1	
MDI002		SD D2	MS D2	XD D2	
MDI003		SD D3	MS D3	XD D3	
MDI004		SD CDM	MS BS	XD WR#	
MDI005		SD CLK	MS CLK	XD CE#	
MDI006		SD RP		XD WP#	
MDI007				XD CLE	
MDI008		NMC D4	MS D4	XD D4	
MDI009		NMC D5	MS D5	XD D5	
MDI010		NMC D6	MS D6	XD D6	
MDI011		NMC D7	MS D7	XD D7	
MDI012				XD RE#	
MDI013				XD R/B#	
MDI014				XD ALE	
CR1 L2D0		SD LED#	MS LED#	XD PWR#	
CR1 PCTLN		SD PWR#	MS PWR#	XD ALE	
CR1 C0D		SD CD#	MS CD#		
CR1 C01					
CR1 C02				XD CD#	

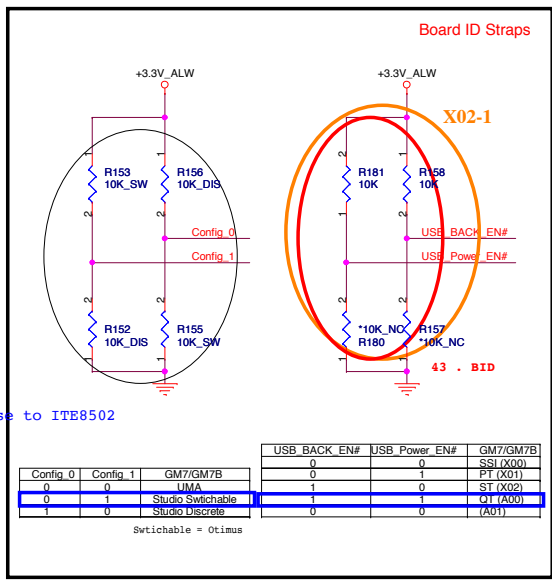
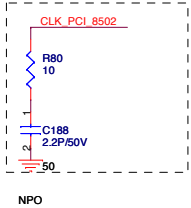
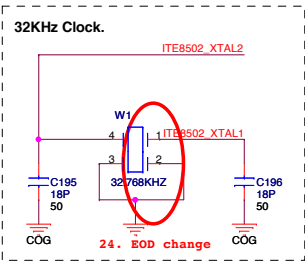
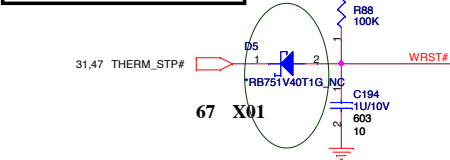
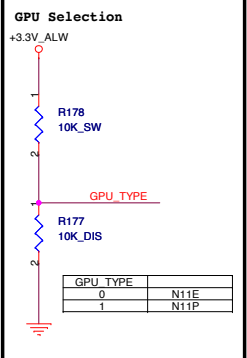




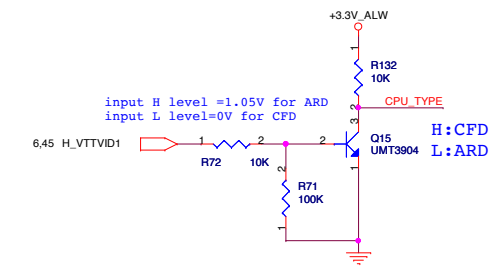
SERIRQ
SC(VI.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k
pull-up to +V3.3S.

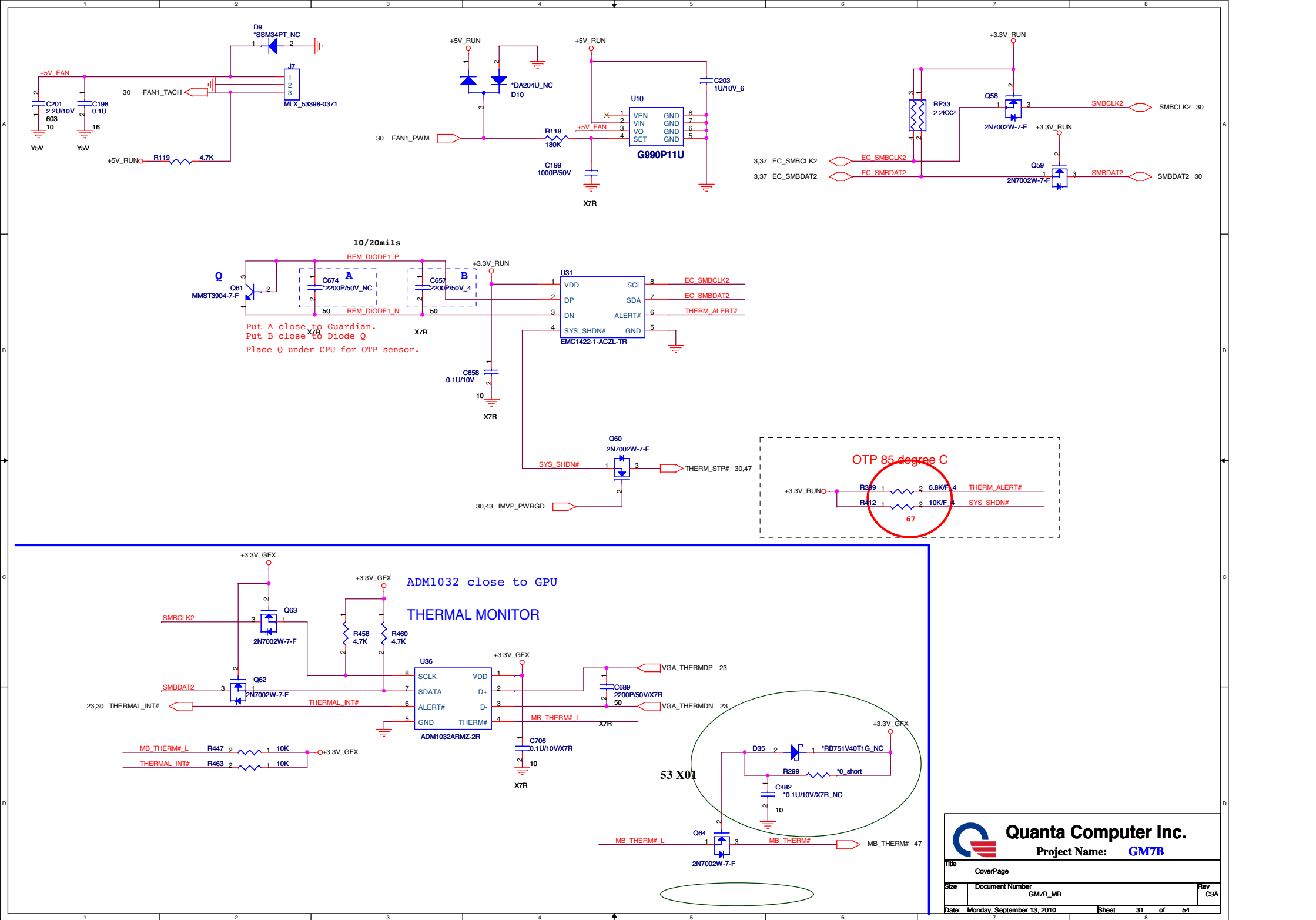
Charge and BAT

PCH CLK, Thermal, VGA Thermal, and MMB

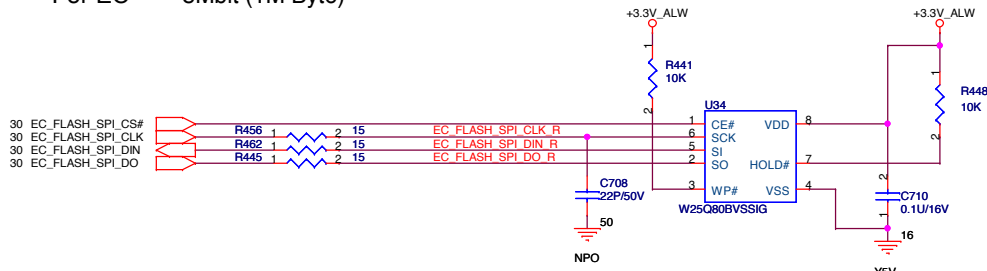


1. Add _SW and _DIS to identify Optimus and DIS only
2. Change board ID to PT



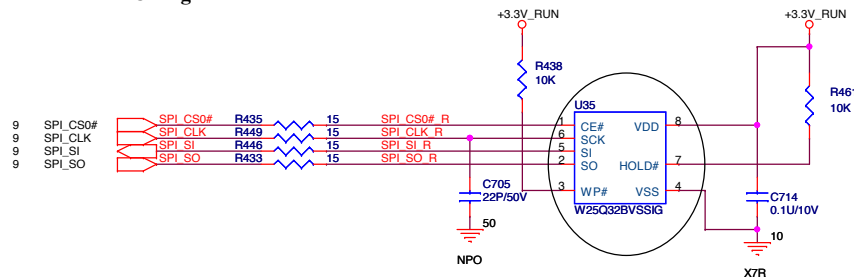


For EC 8Mbit (1M Byte)

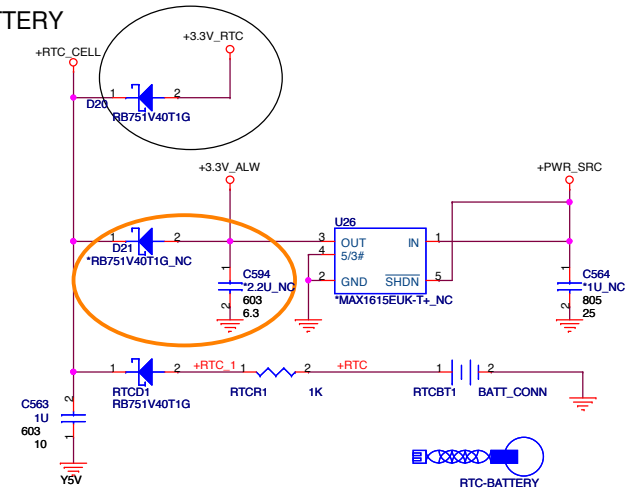


For PCH 32Mbit (4M Byte)

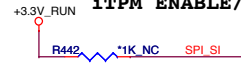
11 X01
0423>Change from 8MB to 4MB



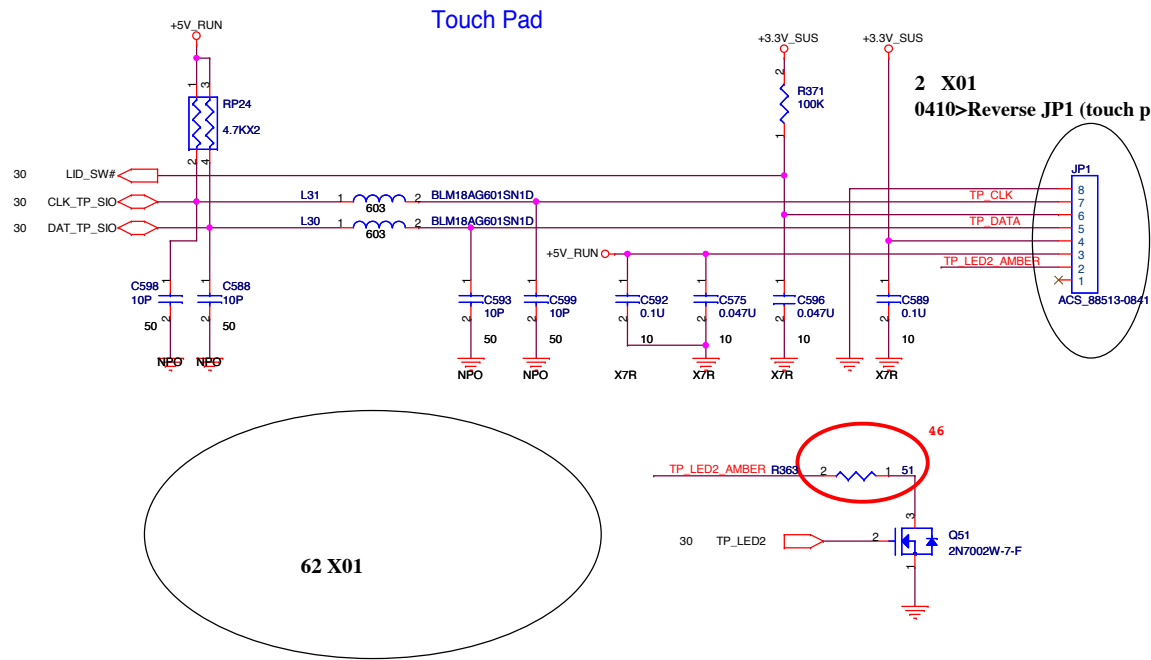
RTC BATTERY



iTPM ENABLE/DISABLE

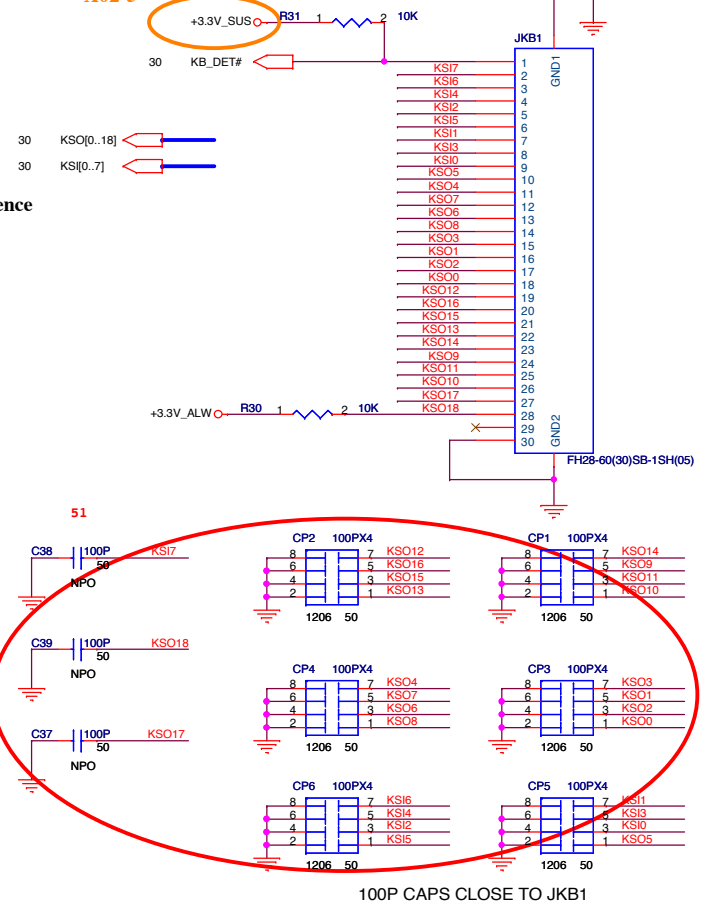


TPM Function	R712
Enable	Mount
Disable	NC (Default)



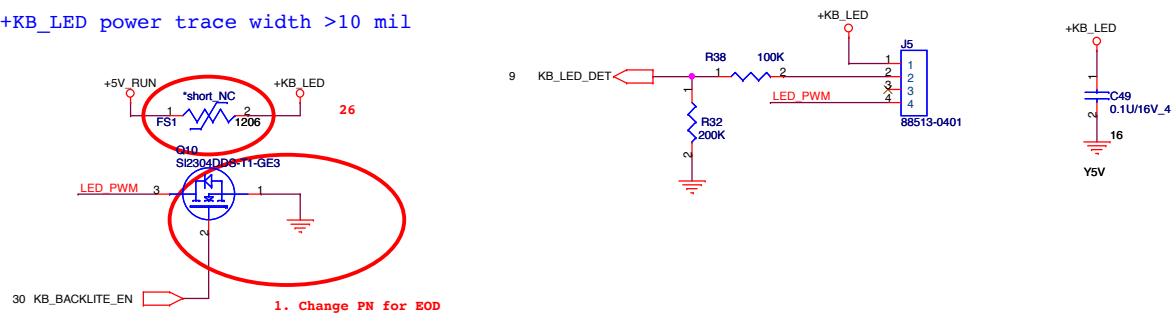
KEYBOARD CONNECTOR

X02-5

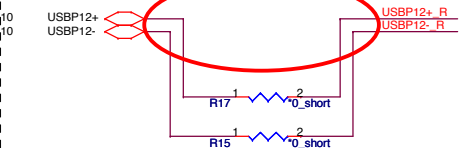
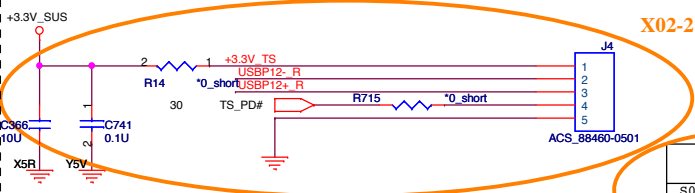


Key board illumination

+KB_LED power trace width >10 mil



Touch Screen Module

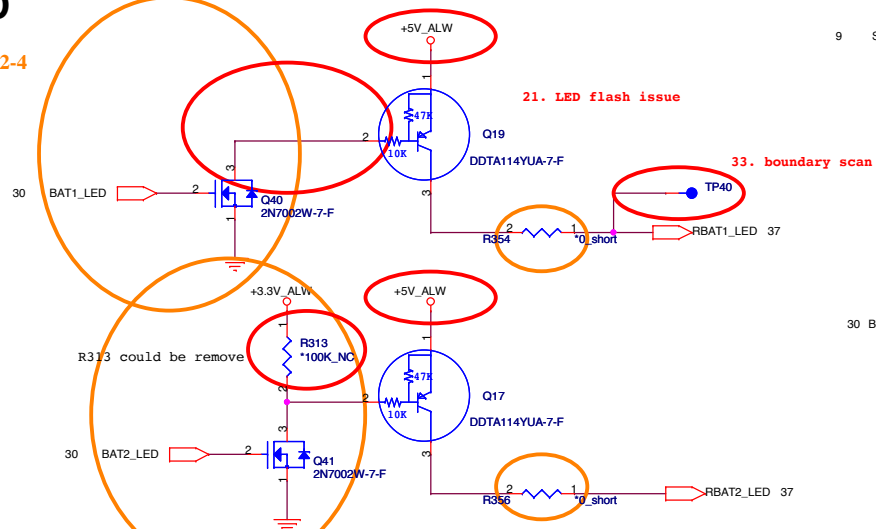


59. delete NC part

LED

X02-4

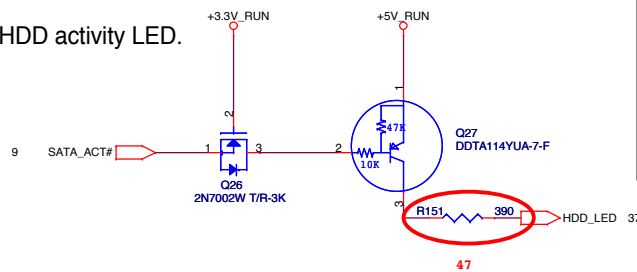
Battery status.



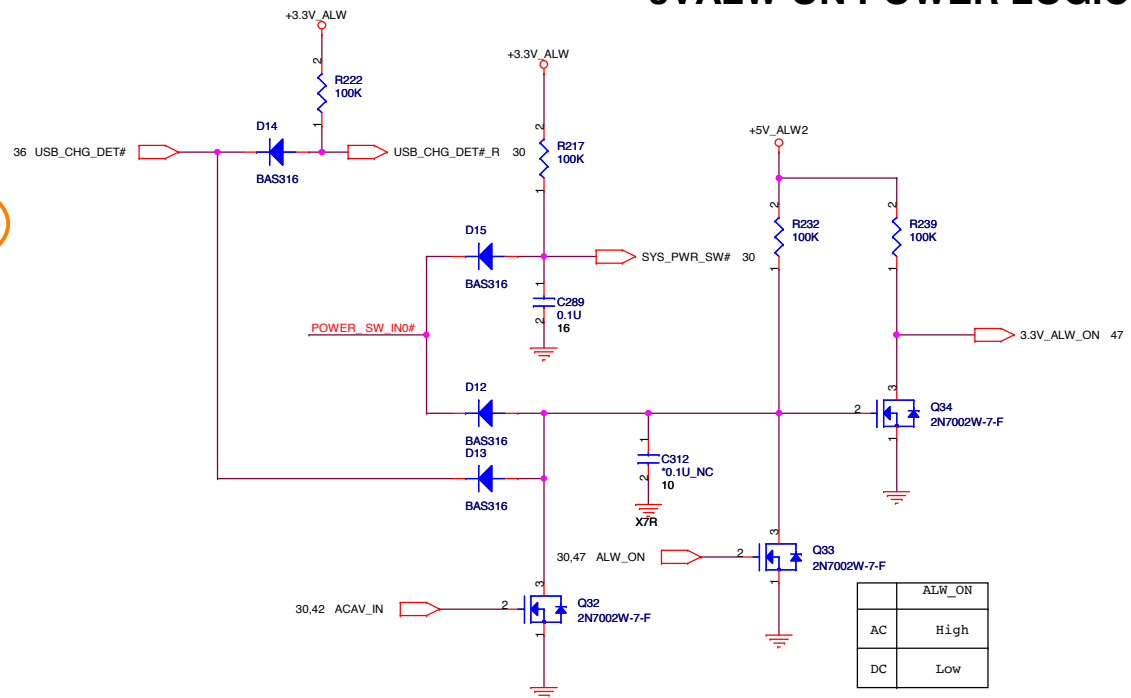
21. LED flash issue

33. boundary scan

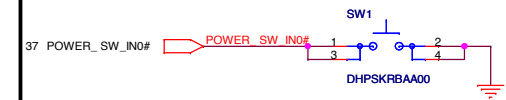
HDD activity LED.



3VALW ON POWER LOGIC



Power button for Engineer

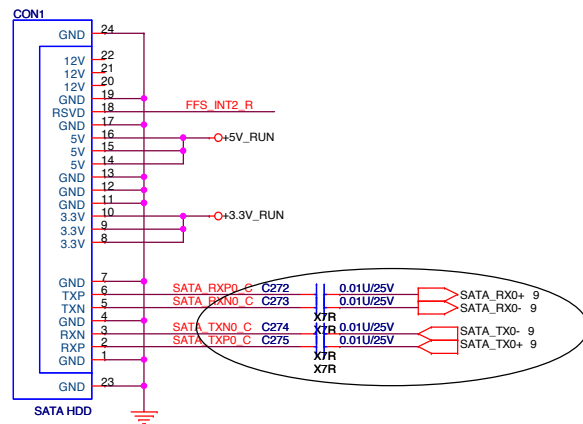


Quanta Computer Inc.

Project Name: **GM7B**

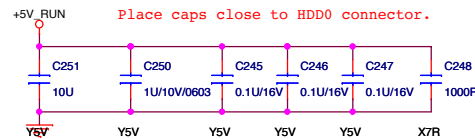
Title		
CoverPage		
Size	Document Number	Rev
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Date: Thursday, September 02, 2010		
Sheet 34 of 54		

HDD0 Connector.

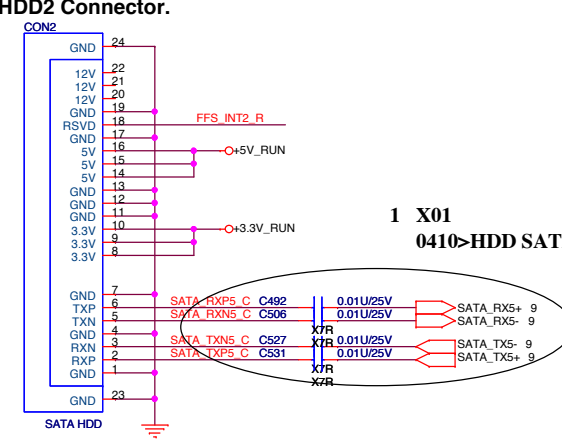


1 X01
0410>HDD SATA TX/RX Reverse

Place caps close to HDD0 connector.

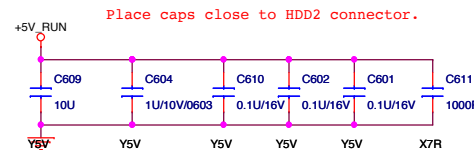


HDD2 Connector.

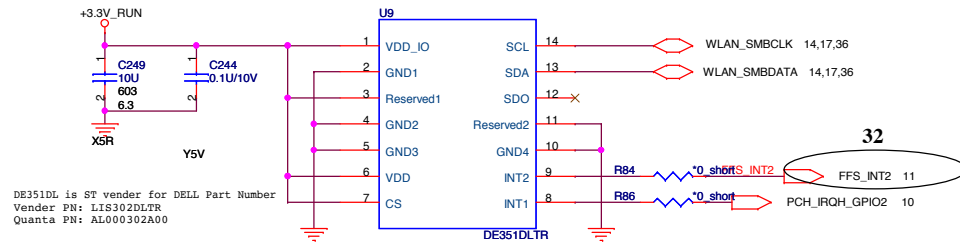


1 X01
0410>HDD SATA TX/RX Reverse

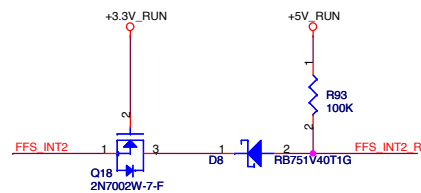
Place caps close to HDD2 connector.



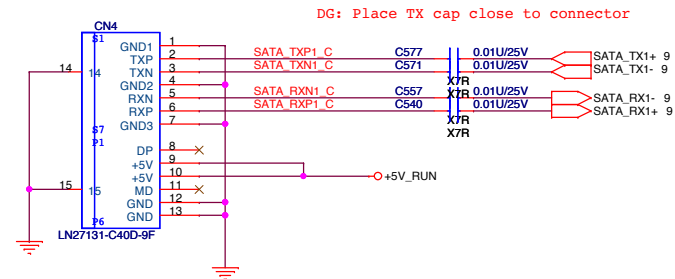
3-axis Fall Sensor (HDD data protector)



DE351DL is ST vender for DELL Part Number
Vender PN: LI8302DLTR
Quanta PN: AL000302A00

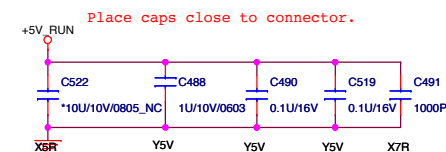


ODD Connector

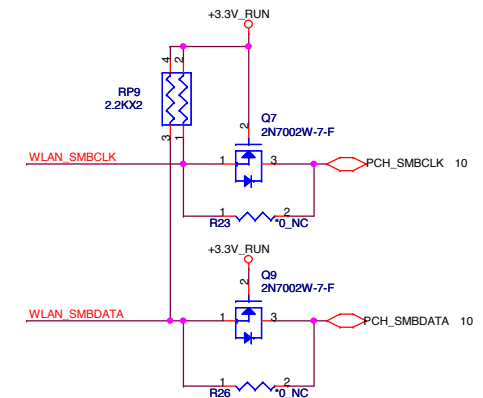
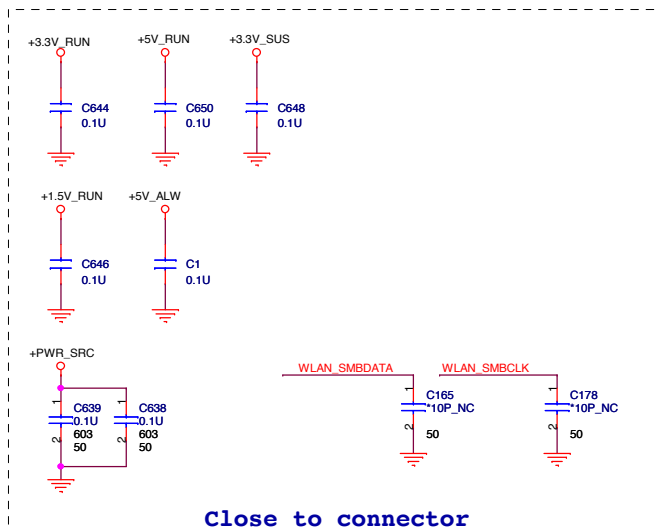
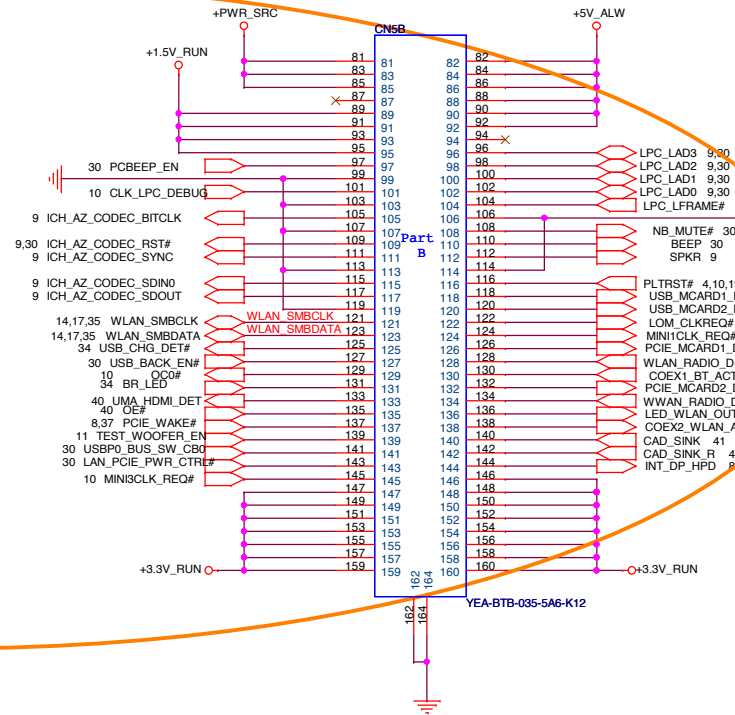
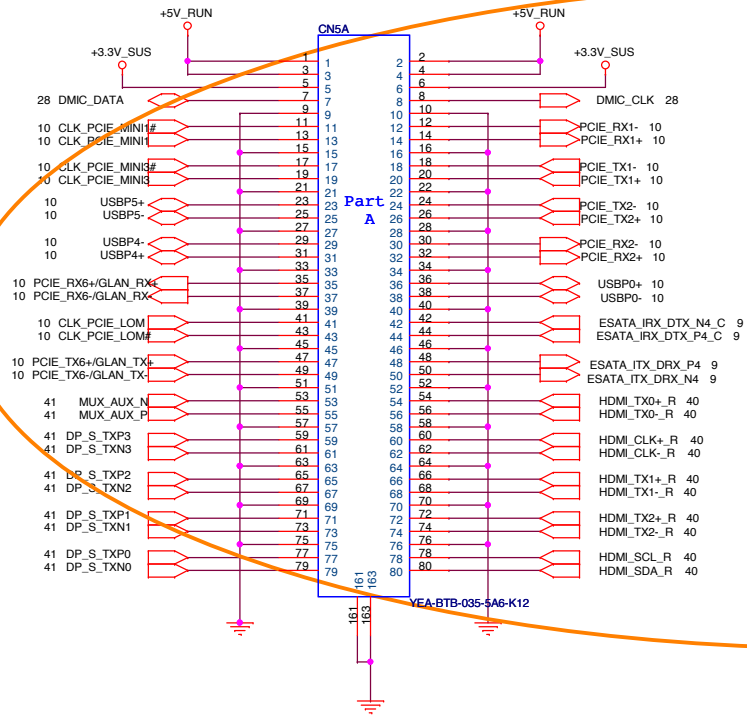


DG: Place TX cap close to connector

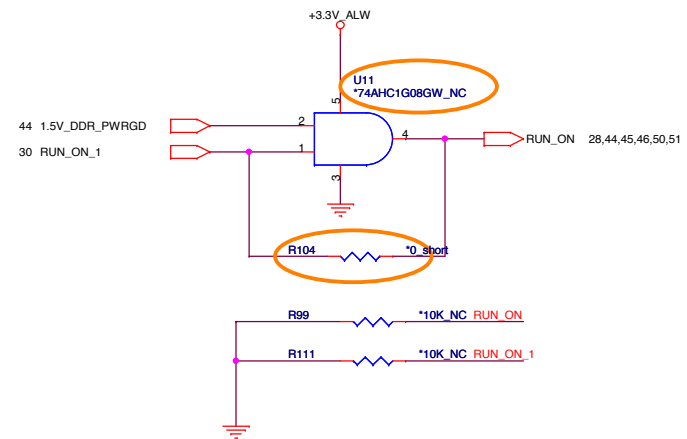
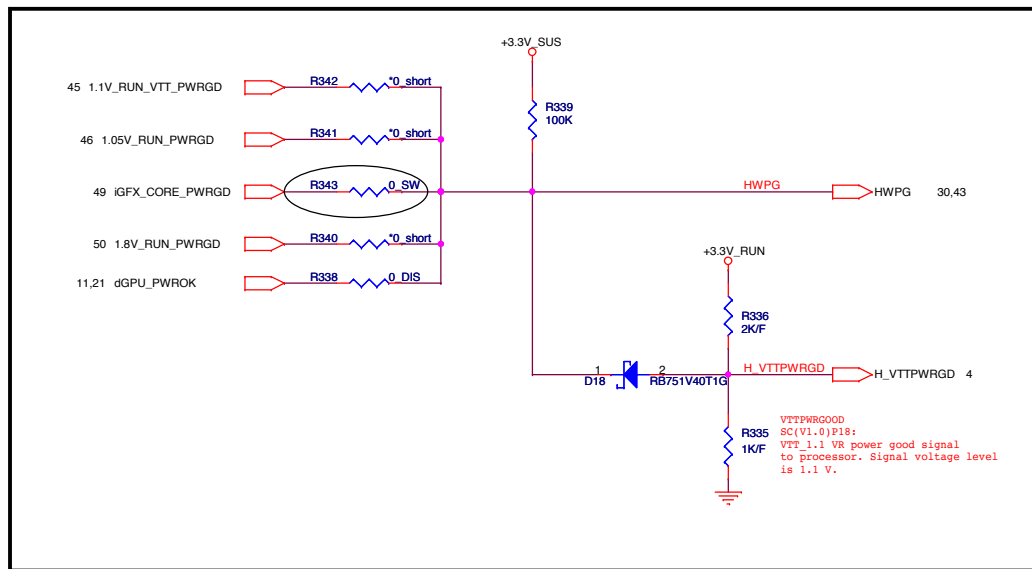
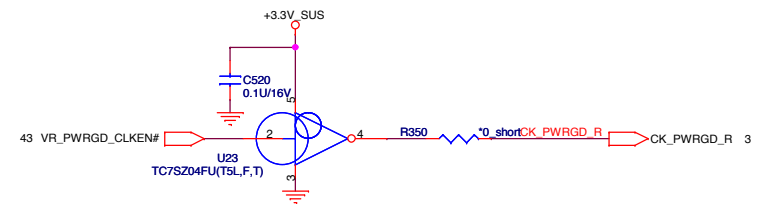
Place caps close to connector.



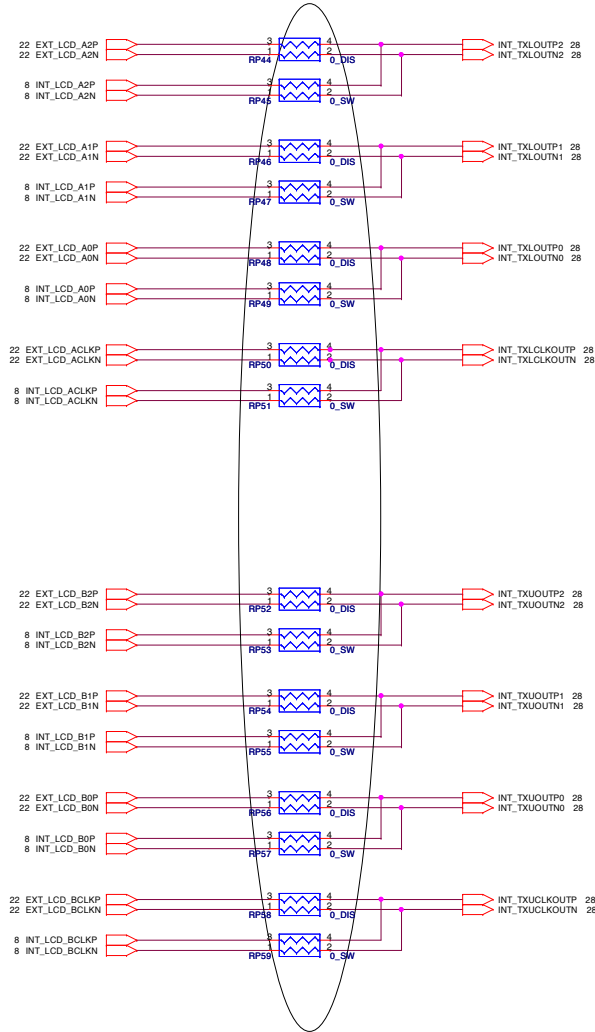
X02-11



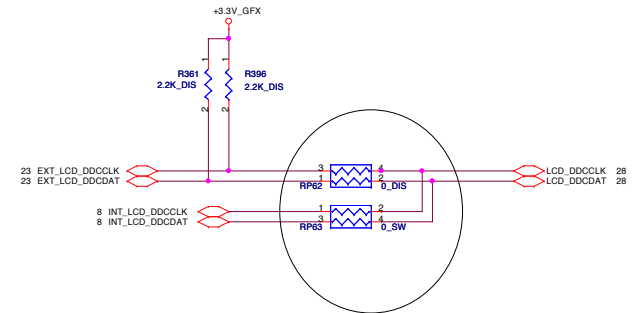
Quanta Computer Inc. Project Name: GM7B		
Title: CoverPage		
Size:	Document Number: GM7B_MB	Rev: C3A
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LVDS Option

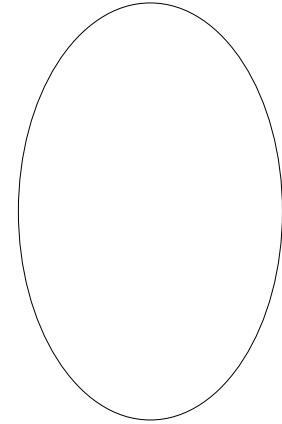


15 X01
0423>Delete MUX and add option resistor

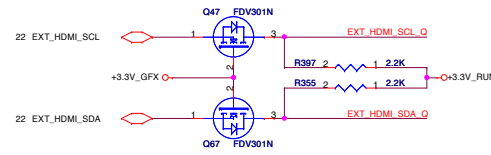


25 X01
0503>Delete circuit for GPU_SELECT

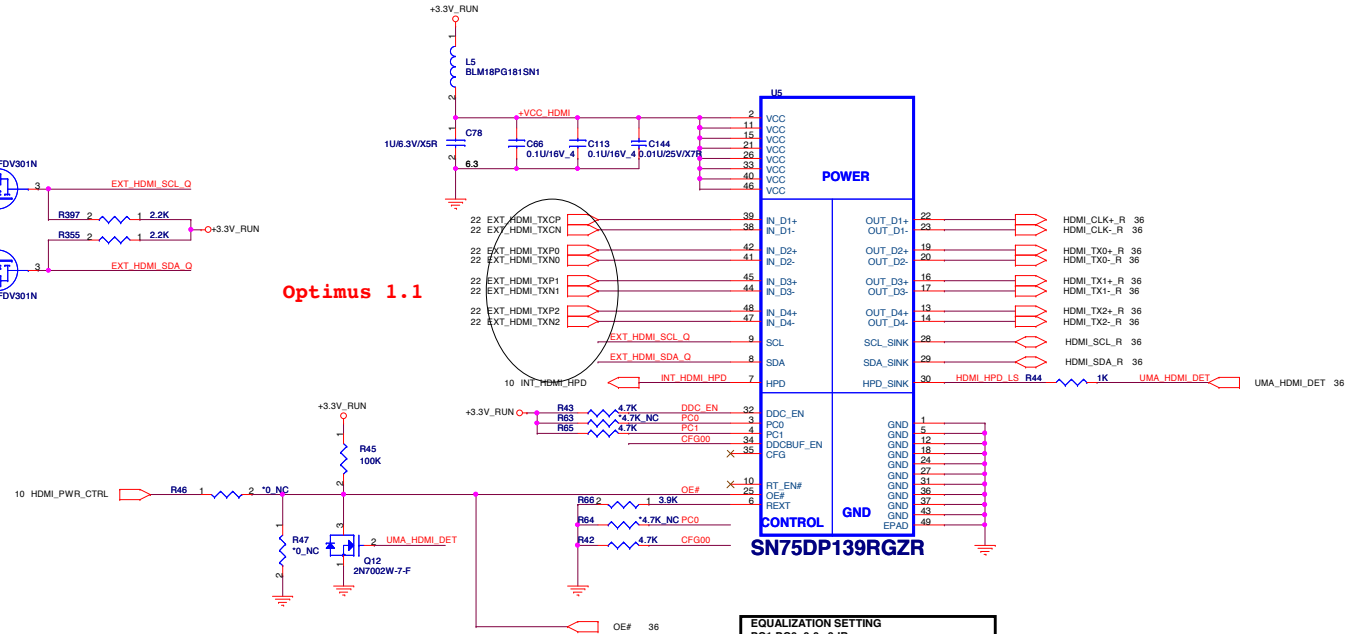
Remove Switch and use option resistor



16 X01
0423>Delete MUX and add option resistor

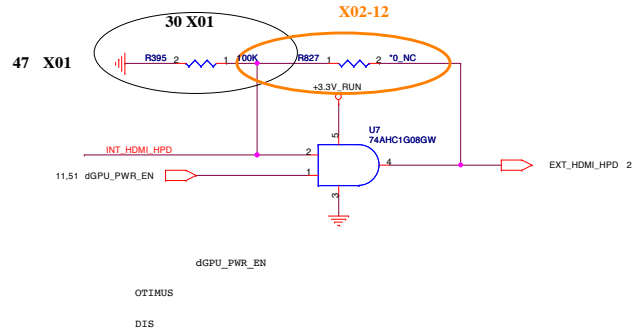


Optimus 1.1

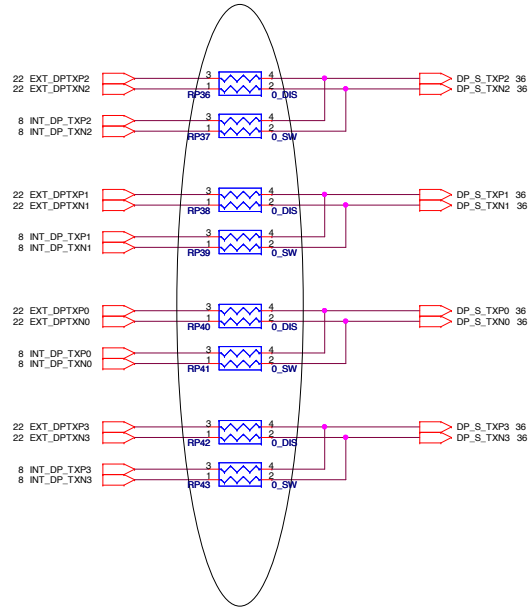


EQUALIZATION SETTING	
PC1:PC0=0:0	8dB
PC1:PC0=0:1	4dB Recommended
PC1:PC0=1:0	12dB
PC1:PC0=1:1	0dB

SCL2/SDA2 Low-level input/output Voltage	
CFG01:CFG00=0:0	VIL:<0.4V VOL:0.6V (Default)
CFG01:CFG00=0:1	VIL:<0.36V VOL:0.55V
CFG01:CFG00=1:0	VIL:<0.44V VOL:0.65V
CFG01:CFG00=1:1	VIL:<0.36V VOL:0.6V



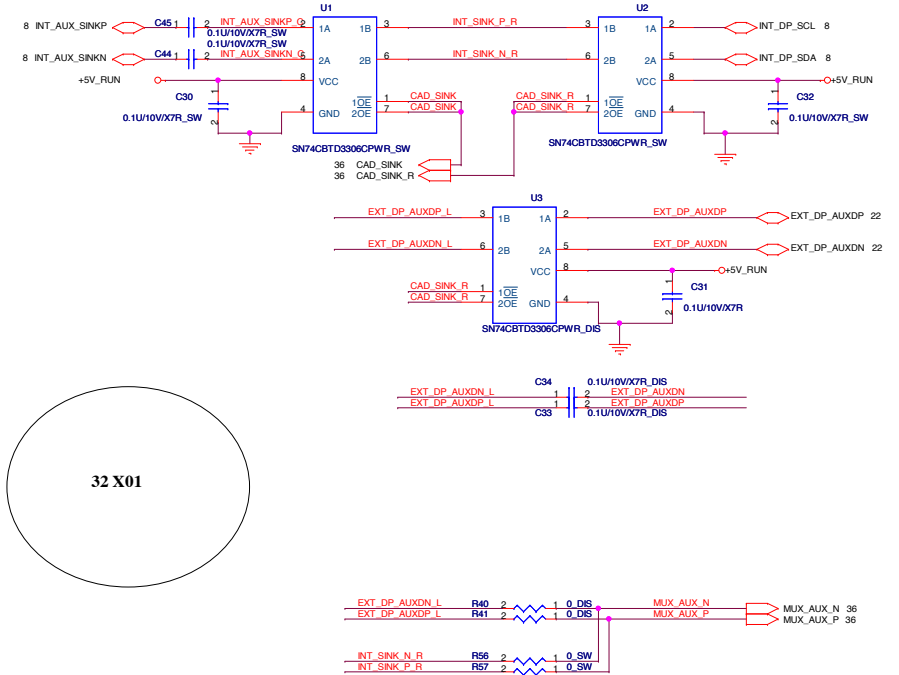
Remove Switch and use option resistor



14 X01

0423>Delete MUX and add option resistor

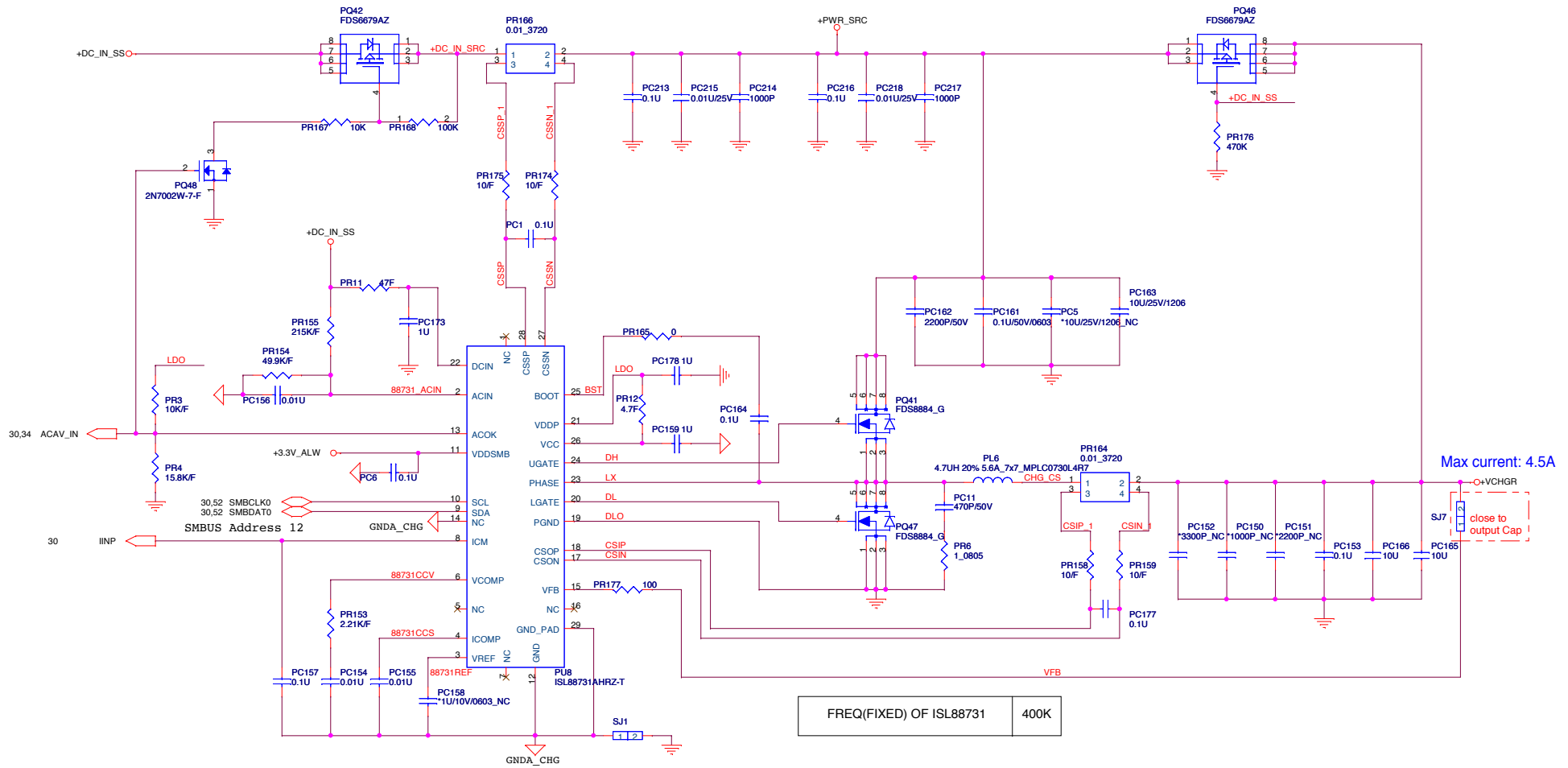
Dual Mode Support



32 X01

dGPU_SELECT	Output
L	DIS only/Hybrid-DIS
H	Optimus/Hybrid-UMA

OE	Output
L	A=B
H	Z

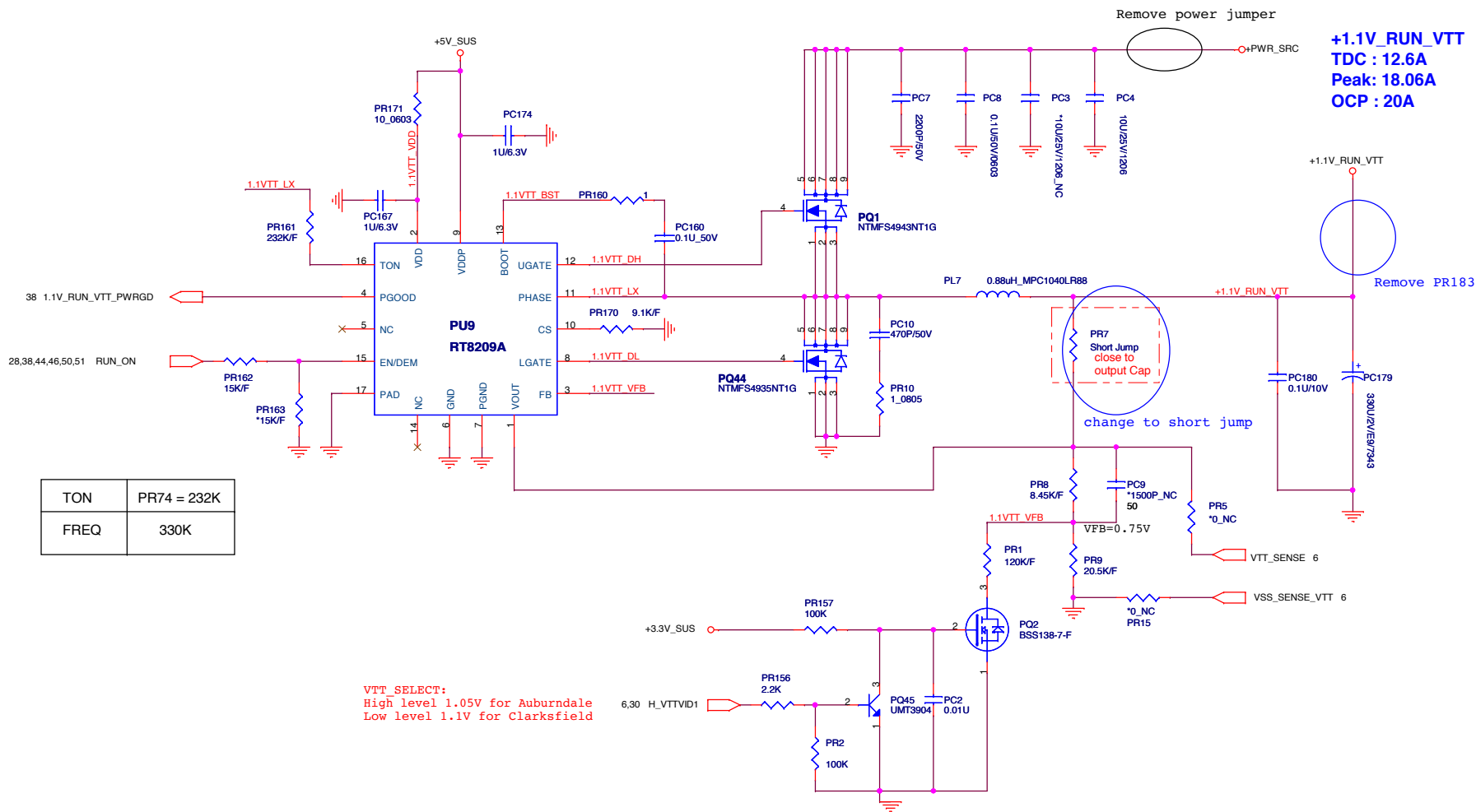


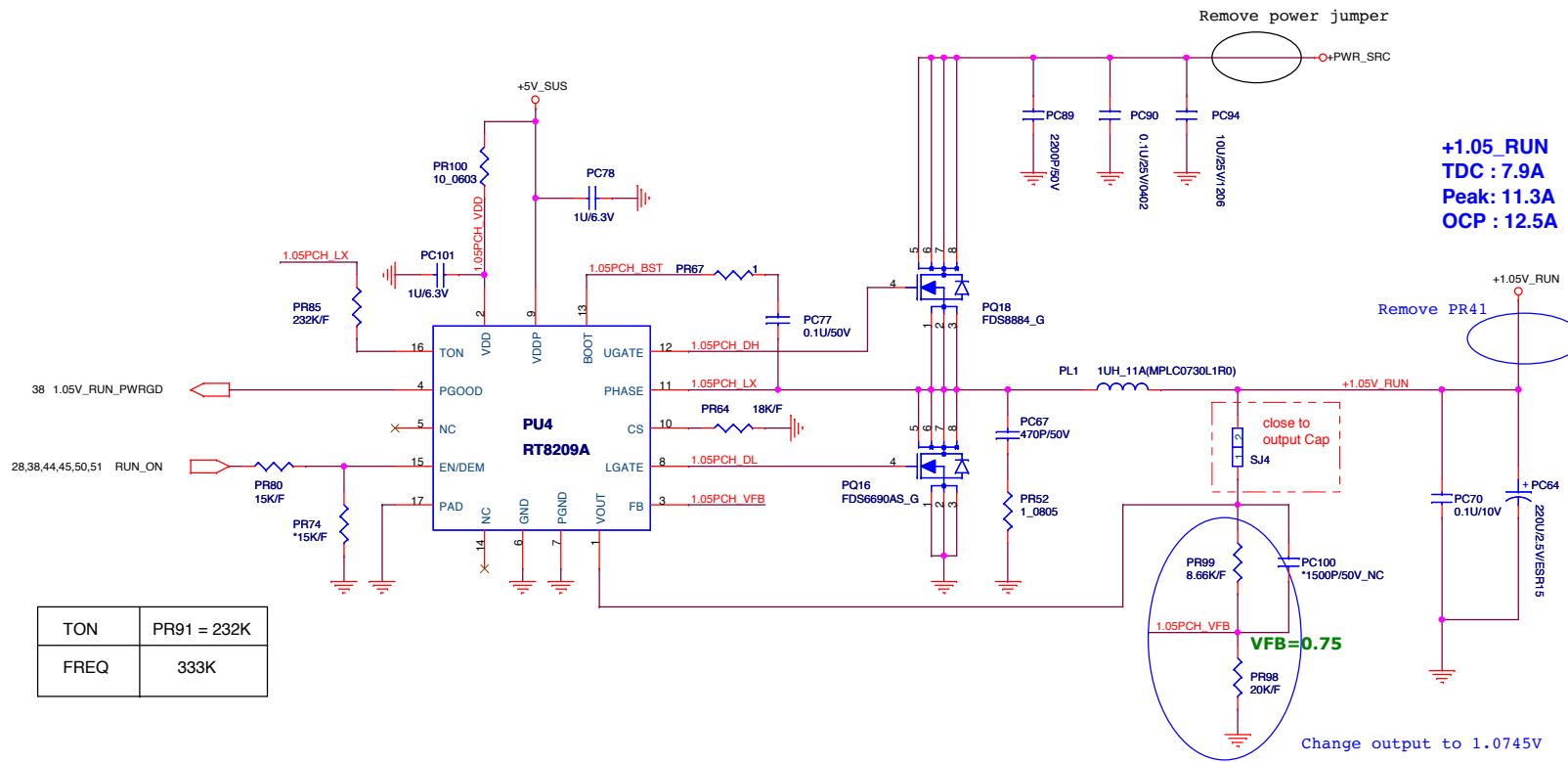
TON	PR67 = 620K
FREQ	400K

VDDQ and VTT discharge control	
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
GND	Non-tracking discharge

VDDQ output voltage selection			
FB	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	0.75V < VDDQ < 3.3V

Outputs Management by S3, S5 control					
State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)





change to short jump

Add PC227, PC228, PC229 for Acoustic Noise

Add PC224, PC225, PC226 for Acoustic Noise

Remove power jumper

+5V_ALW
TDC : 6.6A
Peak: 9.4A
OCP: 10.4A

Remove PR102

change to short jump

TONSEL	OPEN
FREQ	OUT1/400K , OUT2/300K

change to short jump

MB_THERM# 31
PM_THRMTRIP# 4
THERM_STP# 30,31
3.3V_ALW_ON 34

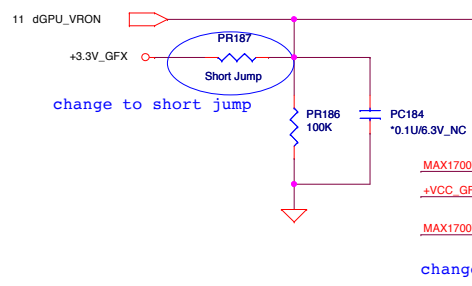
Be NC due to it's no use

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Project Name: **GM7B**

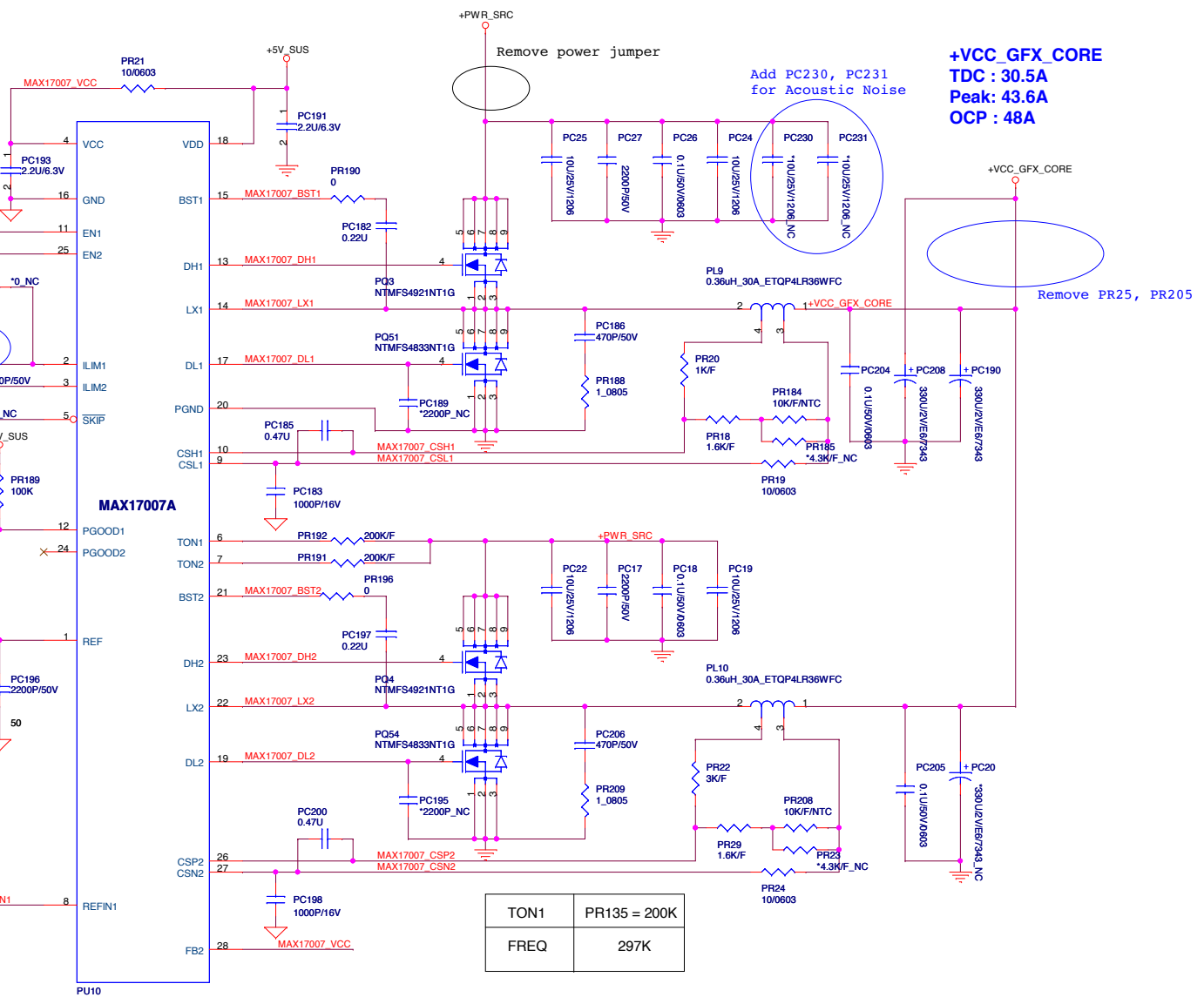
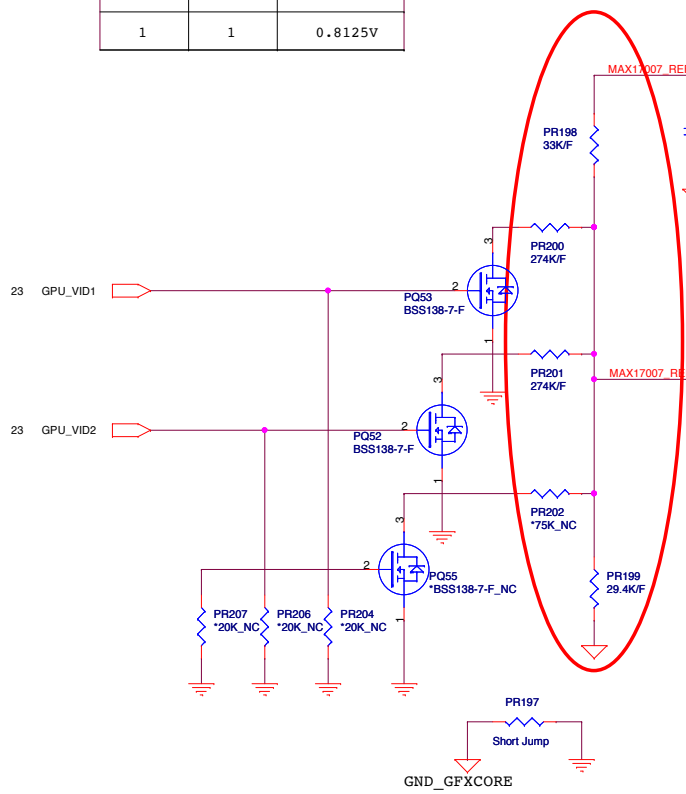
Title: CoverPage

Size: Document Number: GM7B_MB Rev: C3A

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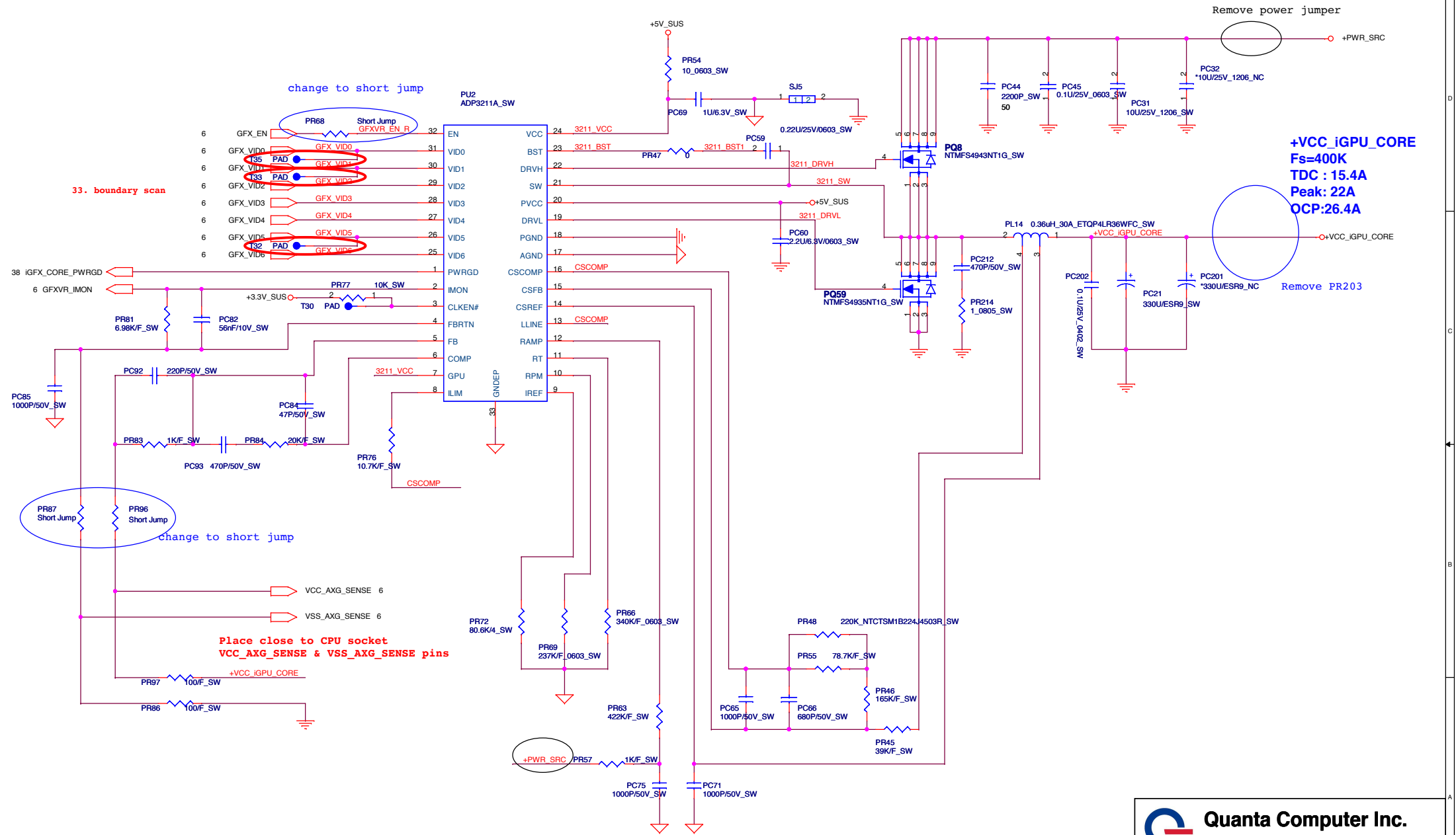


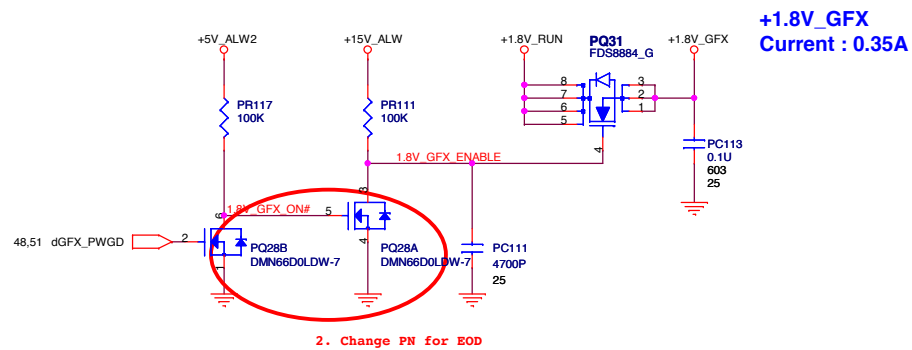
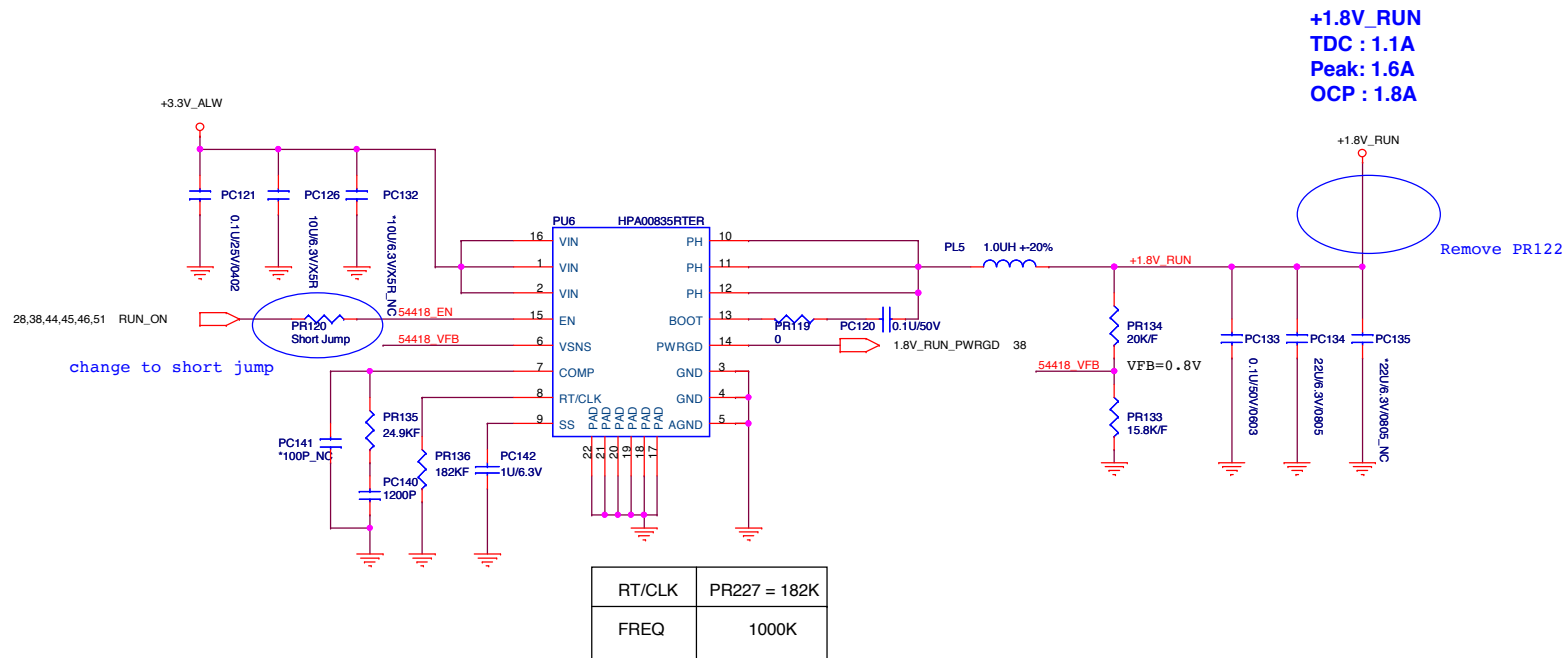
GPU_VID1	GPU_VID2	Voltage
0	0	0.9125V
0	1	0.8625V
1	1	0.8125V

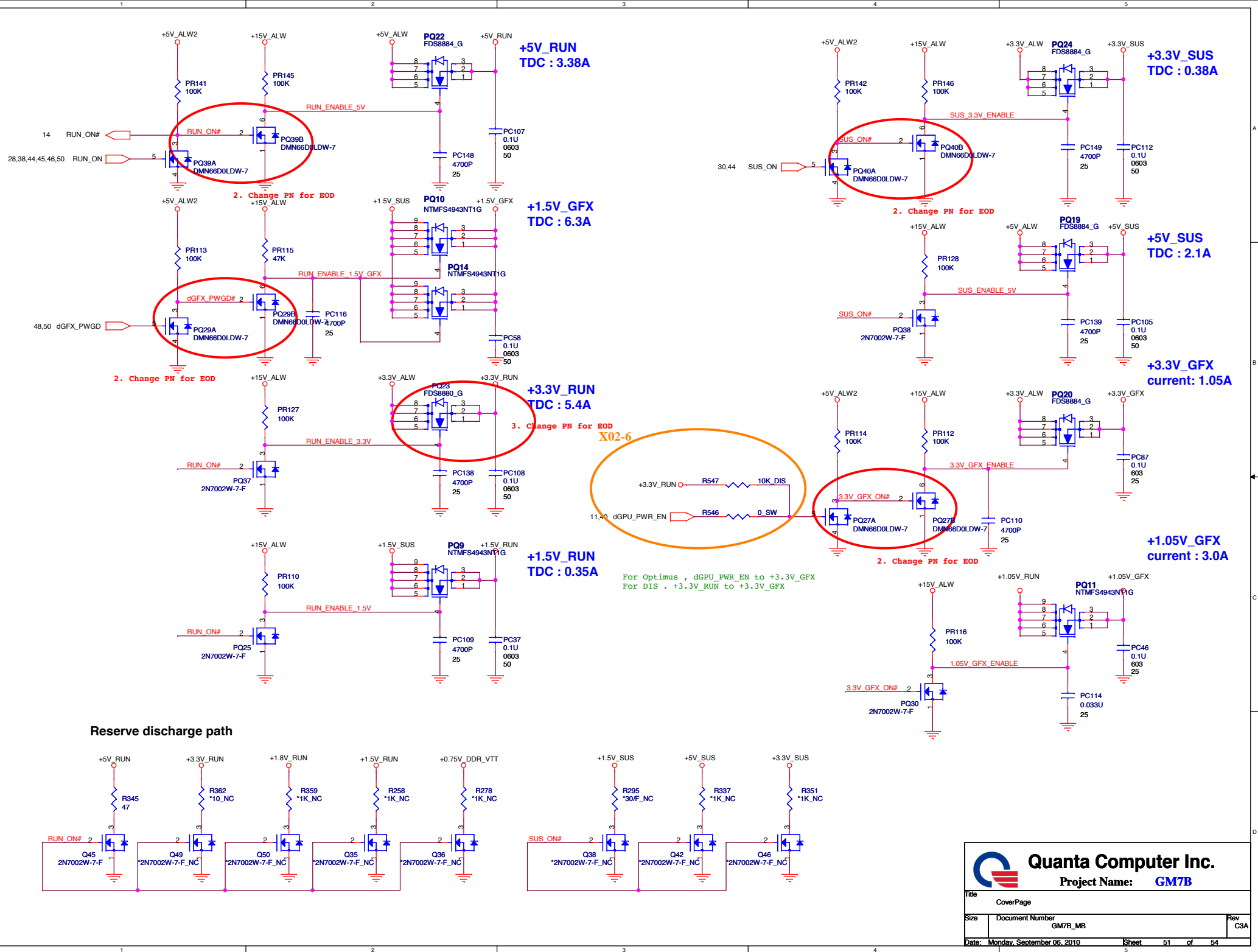


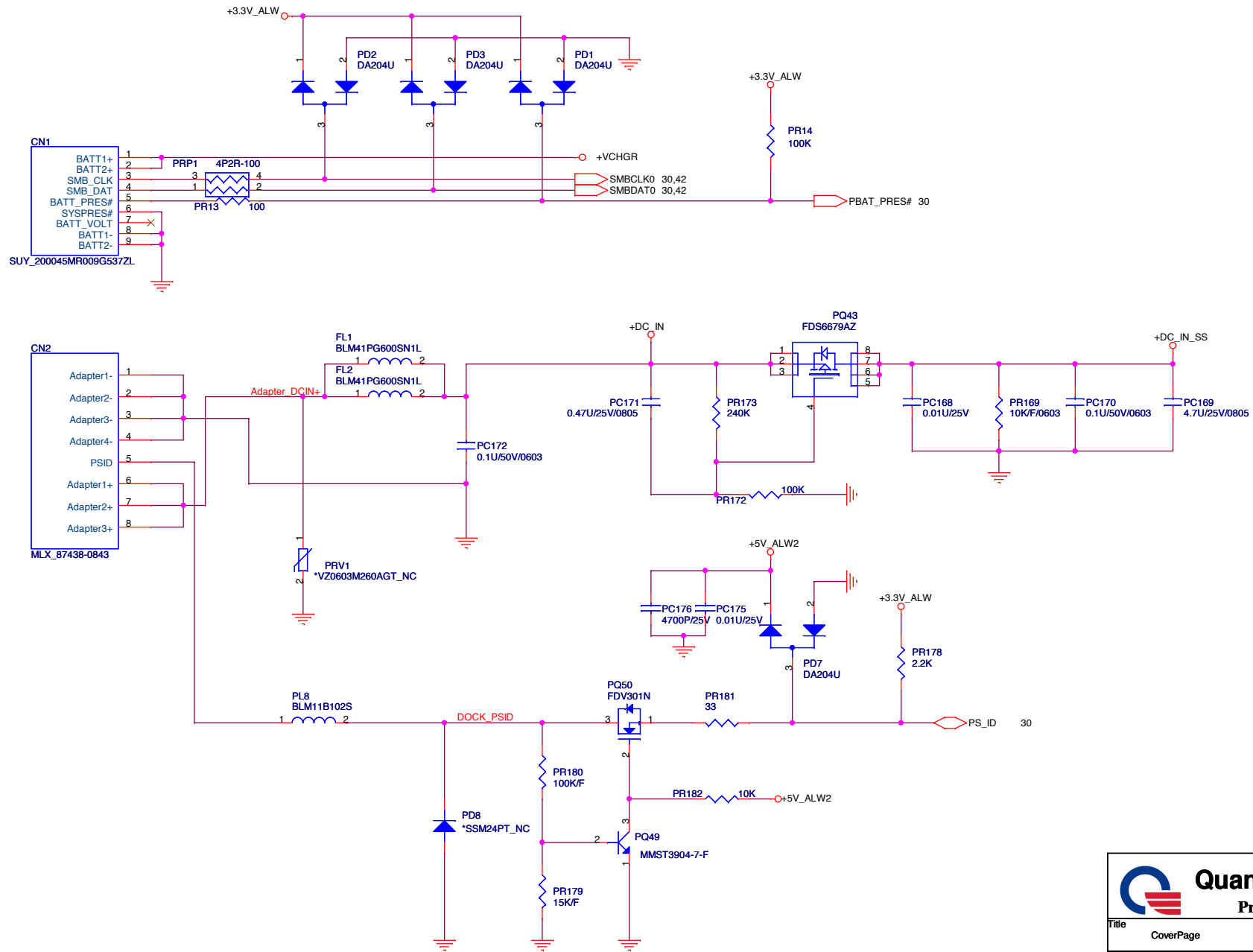
TON1	PR135 = 200K
FREQ	297K

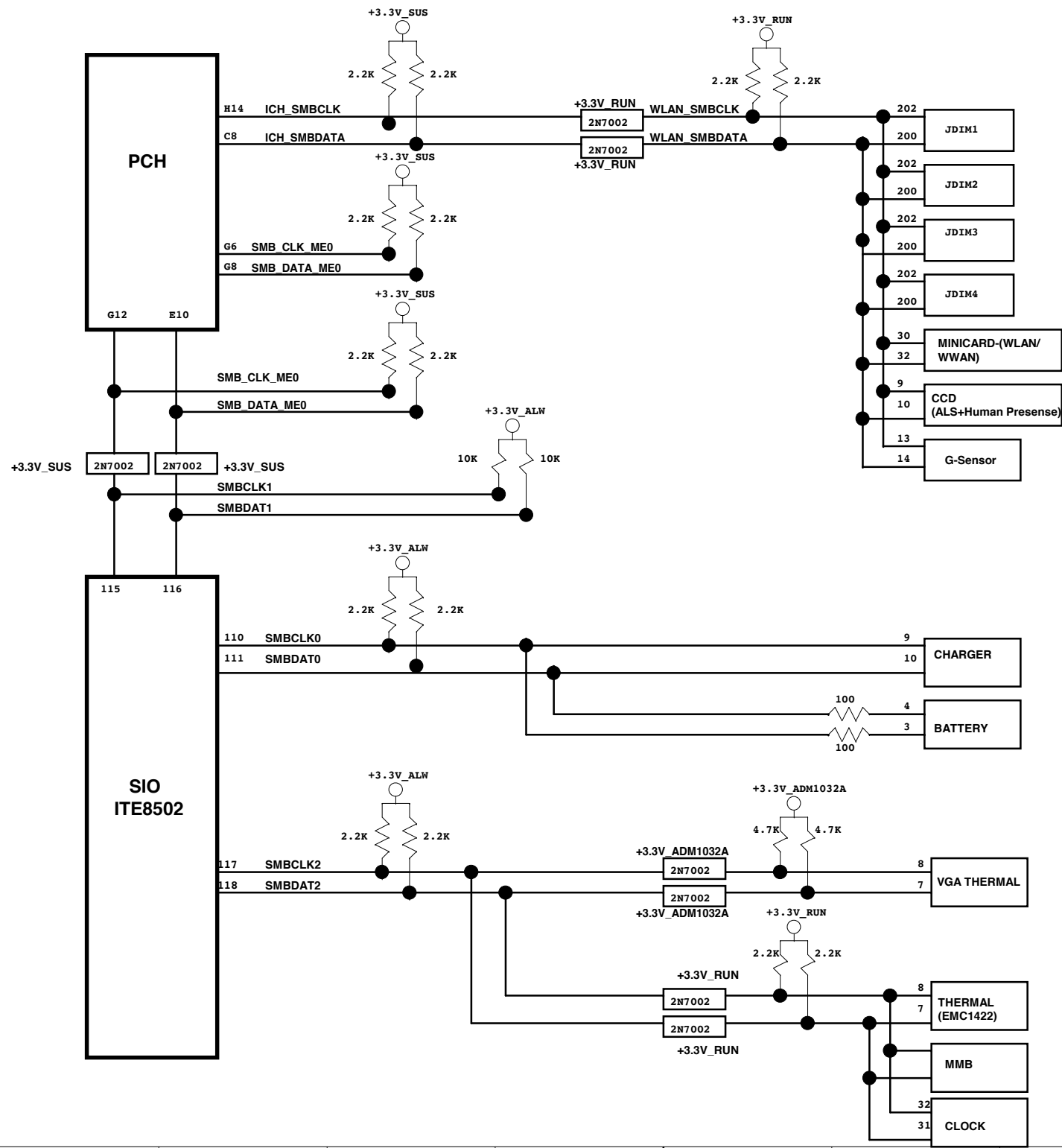
+VCC_GFX_CORE
TDC : 30.5A
Peak: 43.6A
OCP : 48A













34. add label

6. layout change to BOT side

For BTB Use

For CPU Use

